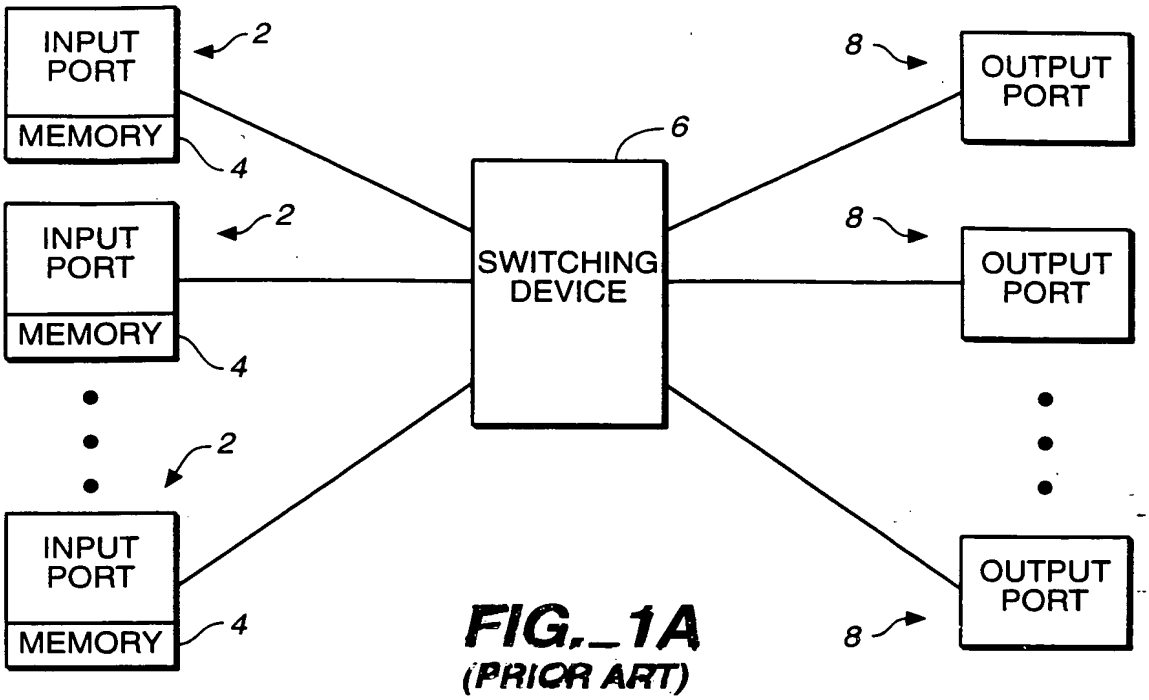


FIG._1A
(PRIOR ART)

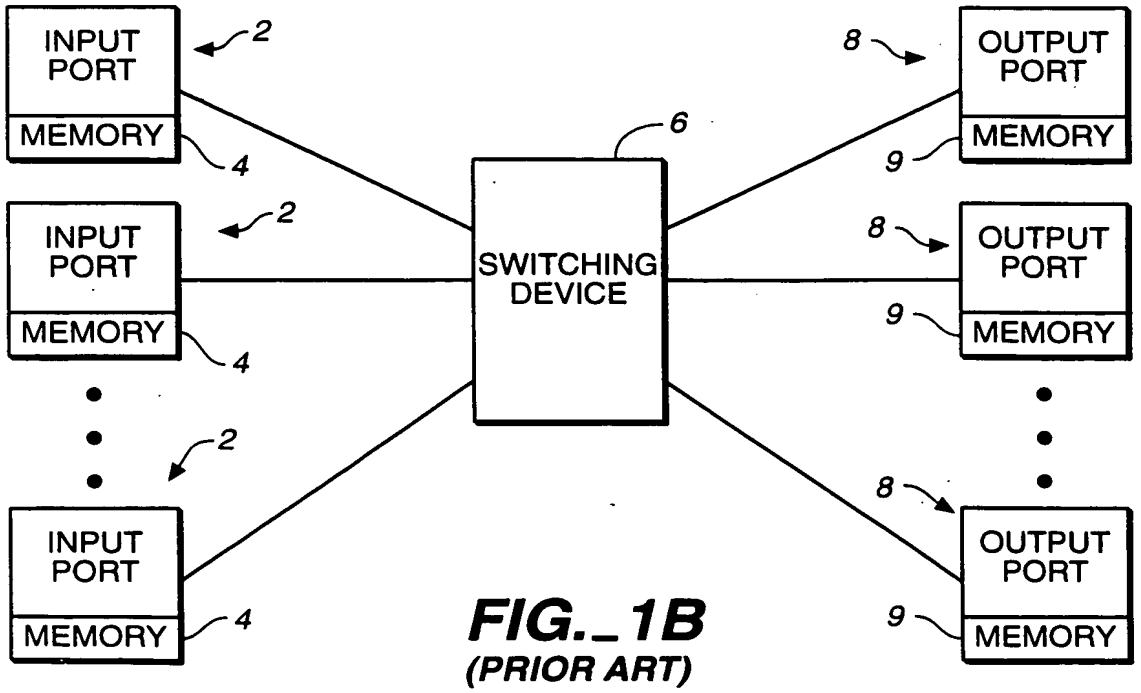


FIG._1B
(PRIOR ART)

SECRET h9859n60

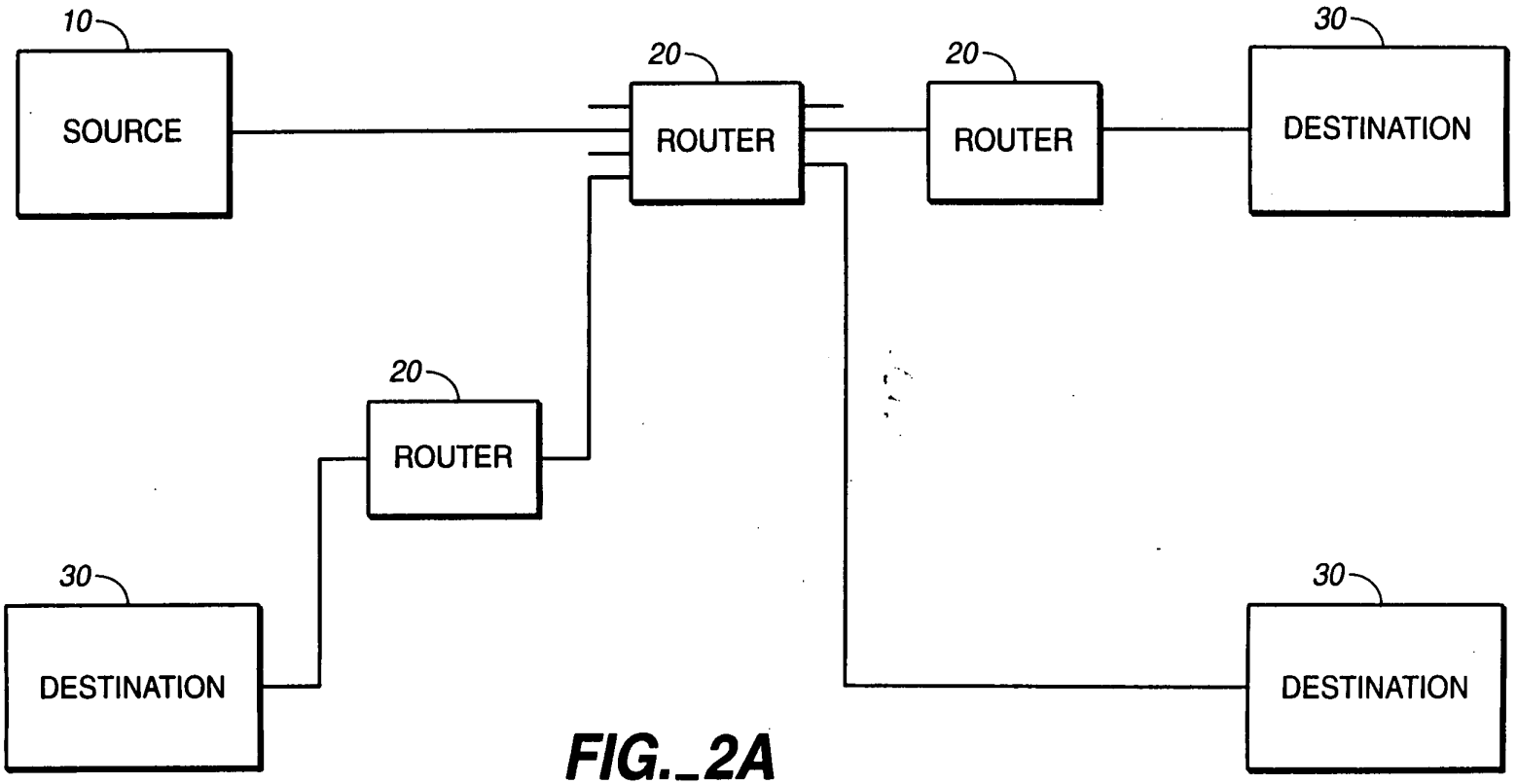


FIG._2A

6627627 H9895H60

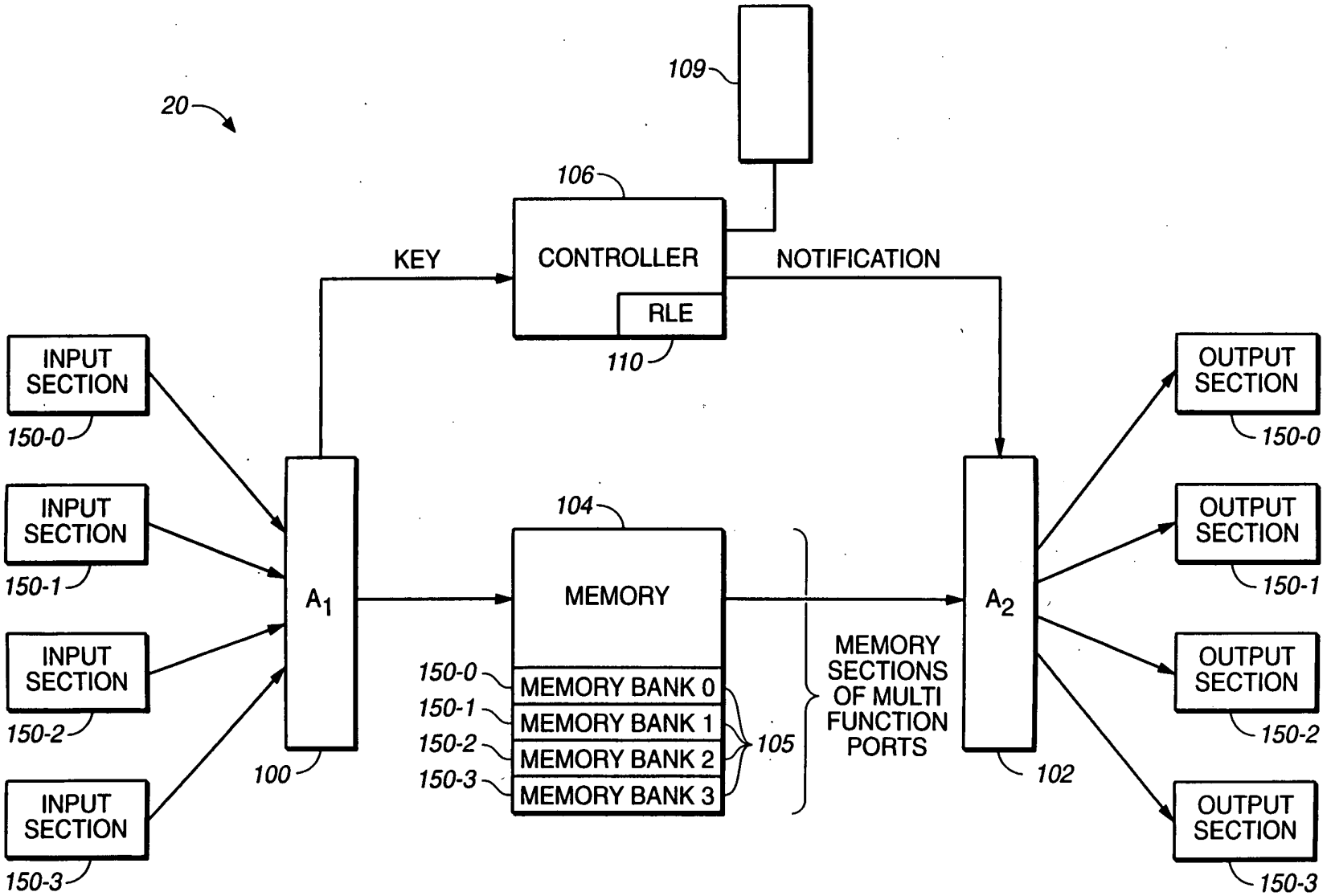


FIG._2B

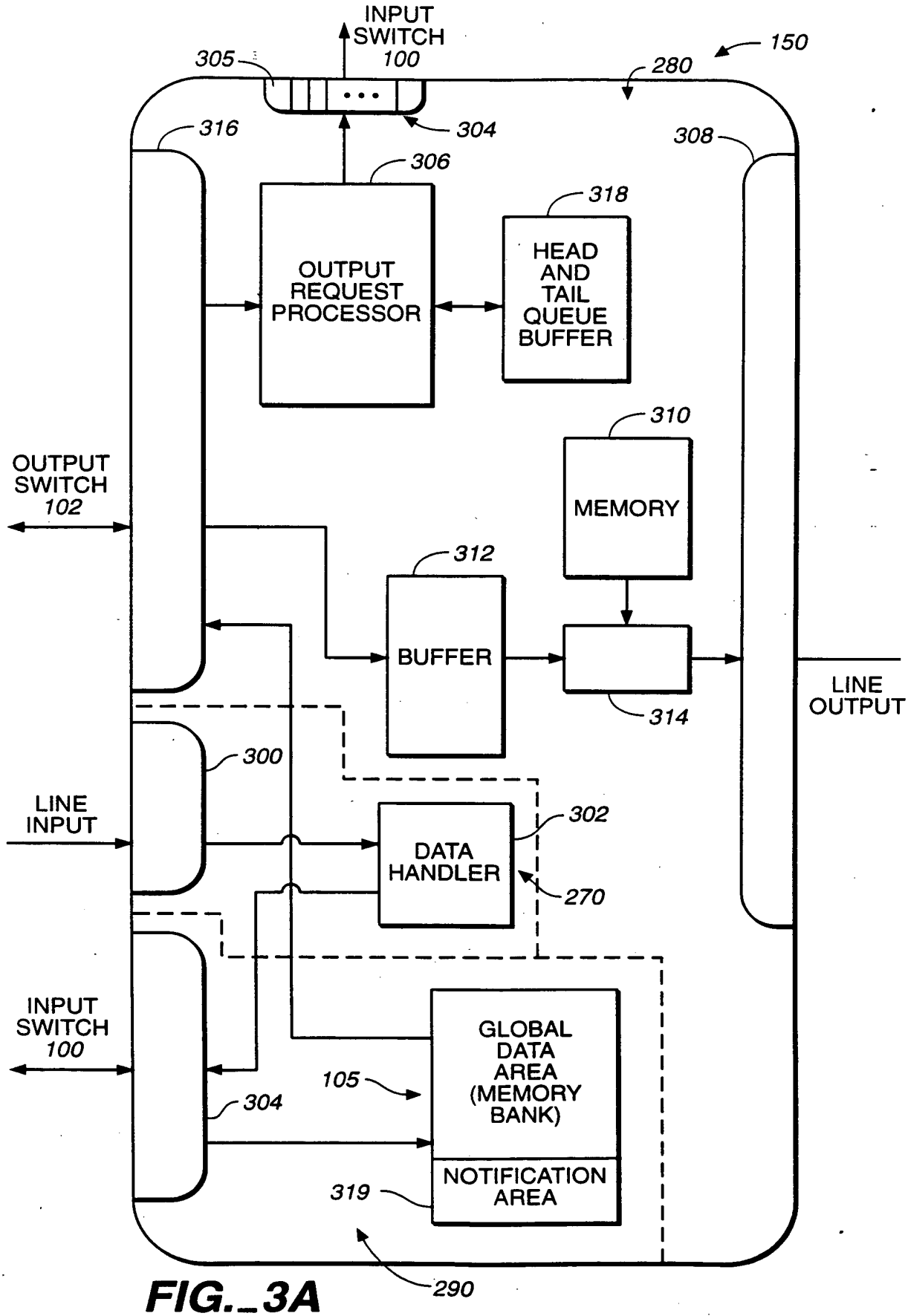

INPUT SWITCH 100
150
305
280
316
304
308
306
318
OUTPUT REQUEST PROCESSOR
HEAD AND TAIL QUEUE BUFFER
310
OUTPUT SWITCH 102
MEMORY
312
BUFFER
314
LINE OUTPUT
300
LINE INPUT
302
DATA HANDLER
270
INPUT SWITCH 100
GLOBAL DATA AREA (MEMORY BANK)
105
304
NOTIFICATION AREA
319
290

FIG._3A

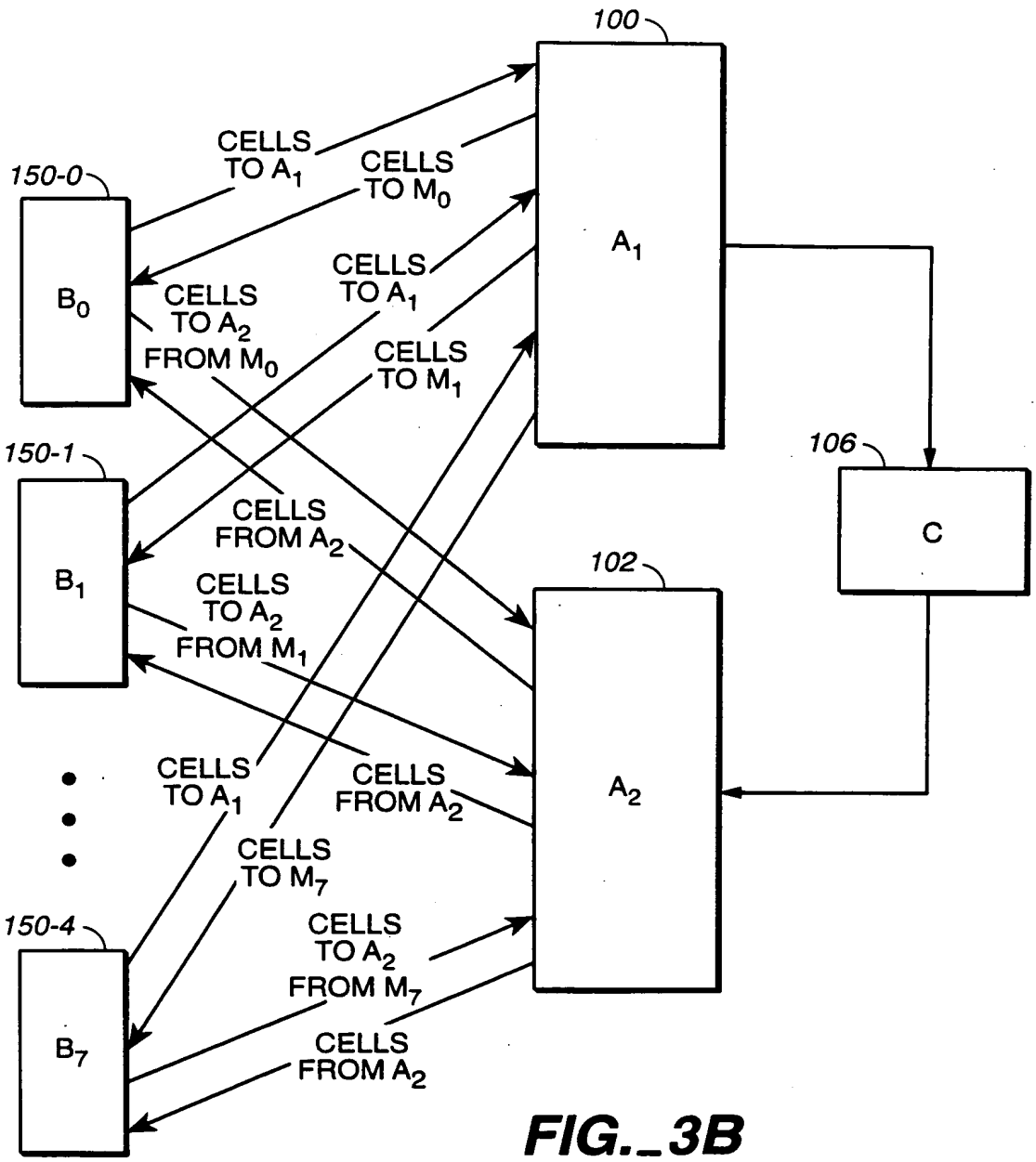

100
150-0
CELLS TO A_1
CELLS TO M_0
B_0
A_1
CELLS TO A_1
CELLS TO A_2 FROM M_0
CELLS TO M_1
150-1
106
C
CELLS FROM A_2
B_1
102
CELLS TO A_2 FROM M_1
A_2
CELLS TO A_1
CELLS FROM A_2
CELLS TO M_7
150-4
CELLS TO A_2 FROM M_7
B_7
CELLS FROM A_2

FIG._3B

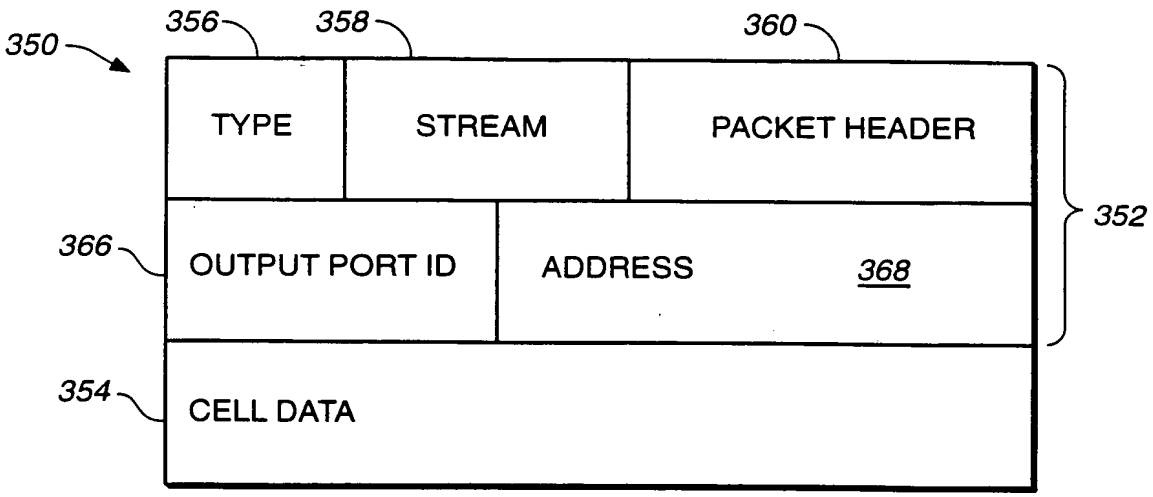

350
356
358
360
TYPE
STREAM
PACKET HEADER
352
366
OUTPUT PORT ID
ADDRESS
368
354
CELL DATA

FIG._3C

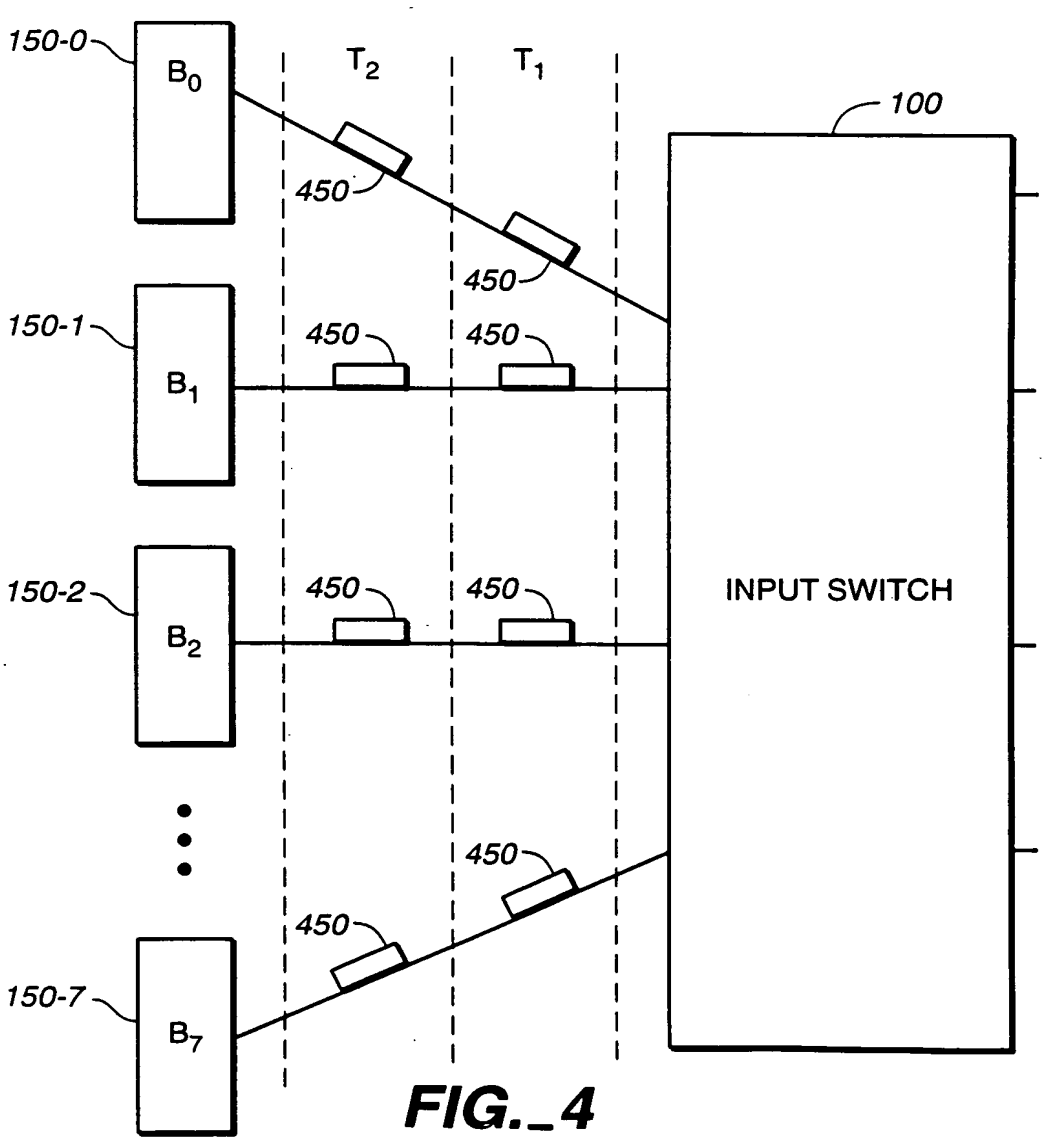

150-0
B0
T2
T1
100
450
450
150-1
B1
450
450
150-2
B2
450
450
INPUT SWITCH
450
450
150-7
B7

FIG._4

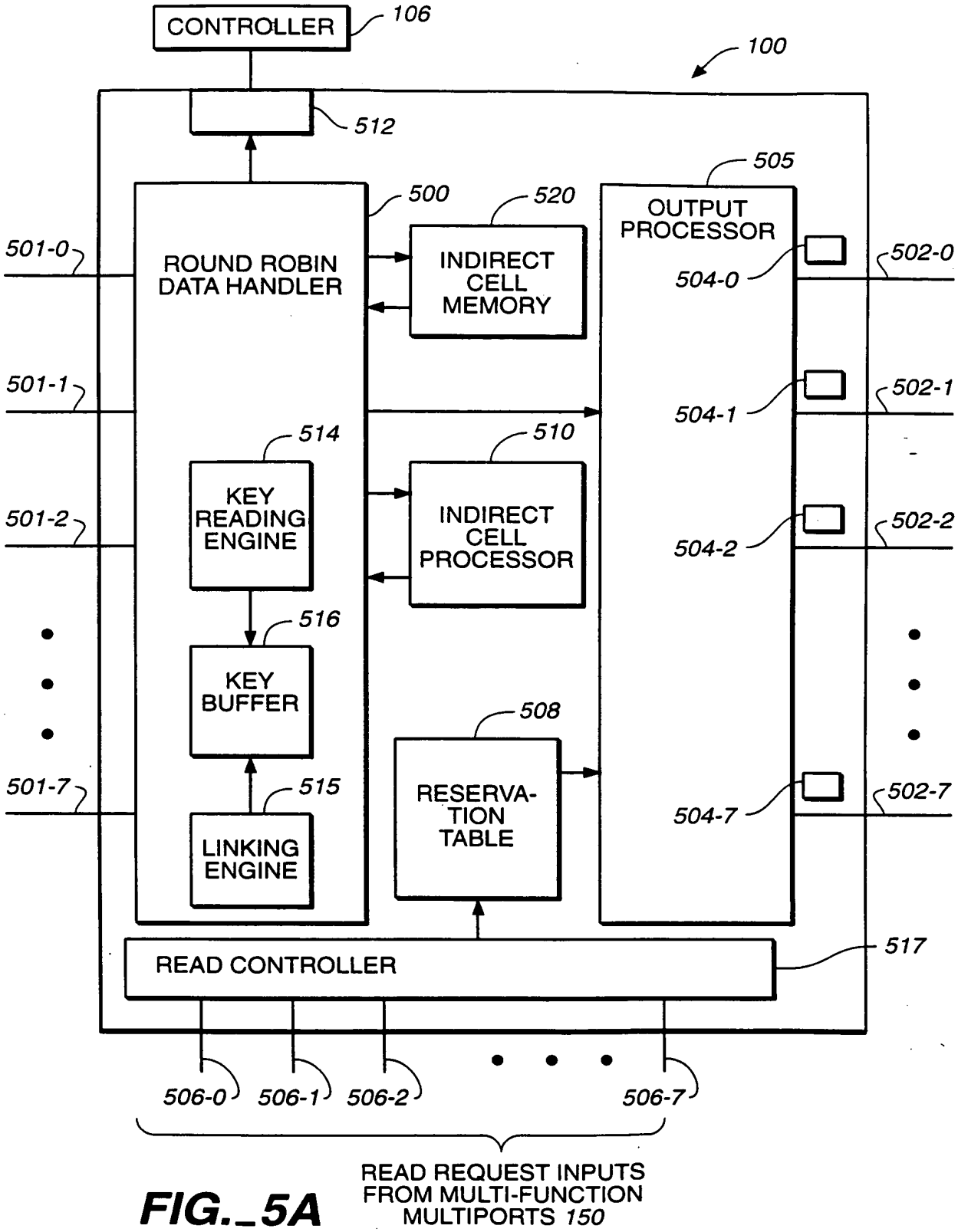

CONTROLLER
106
100
512
505
500
520
OUTPUT PROCESSOR
501-0
ROUND ROBIN DATA HANDLER
INDIRECT CELL MEMORY
504-0
502-0
501-1
504-1
502-1
514
510
KEY READING ENGINE
INDIRECT CELL PROCESSOR
501-2
504-2
502-2
516
KEY BUFFER
508
501-7
515
RESERVA-TION TABLE
504-7
502-7
LINKING ENGINE
517
READ CONTROLLER
506-0
506-1
506-2
506-7
READ REQUEST INPUTS FROM MULTI-FUNCTION MULTIPORTS 150

FIG._5A

6627271 1999960

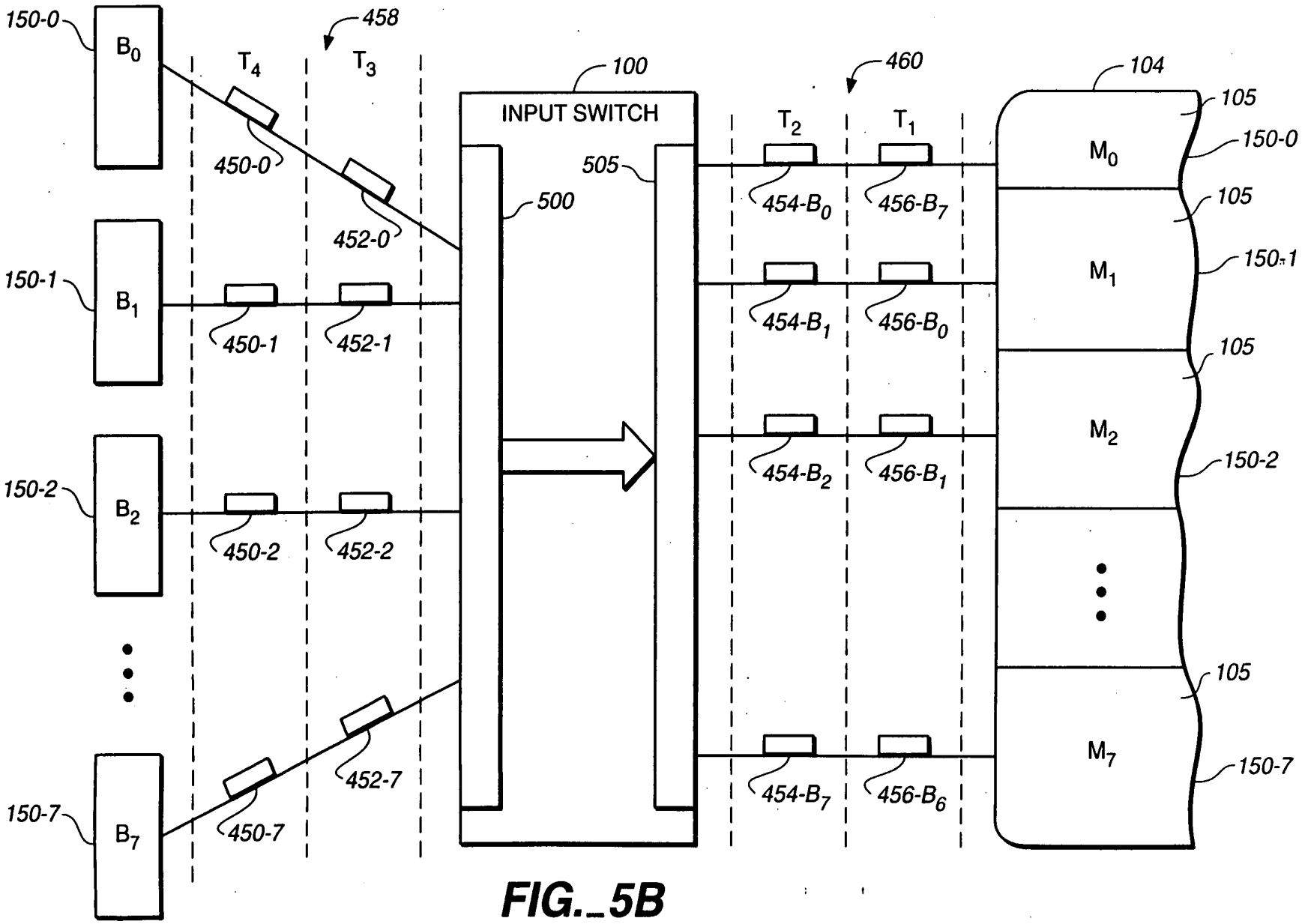


FIG._5B

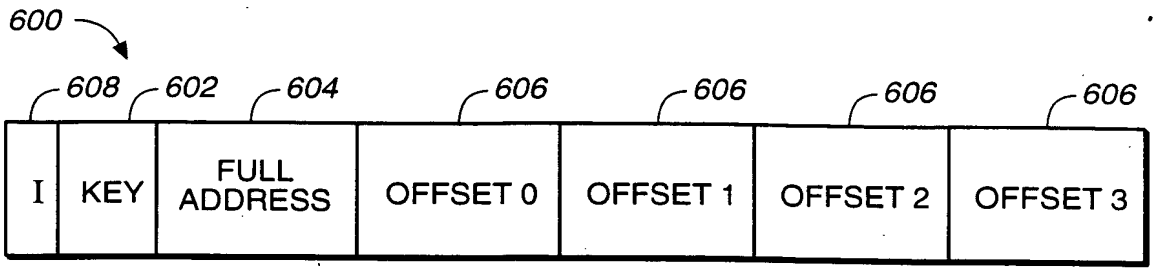

600
608
602
604
606
606
606
606
I
KEY
FULL ADDRESS
OFFSET 0
OFFSET 1
OFFSET 2
OFFSET 3

FIG._6

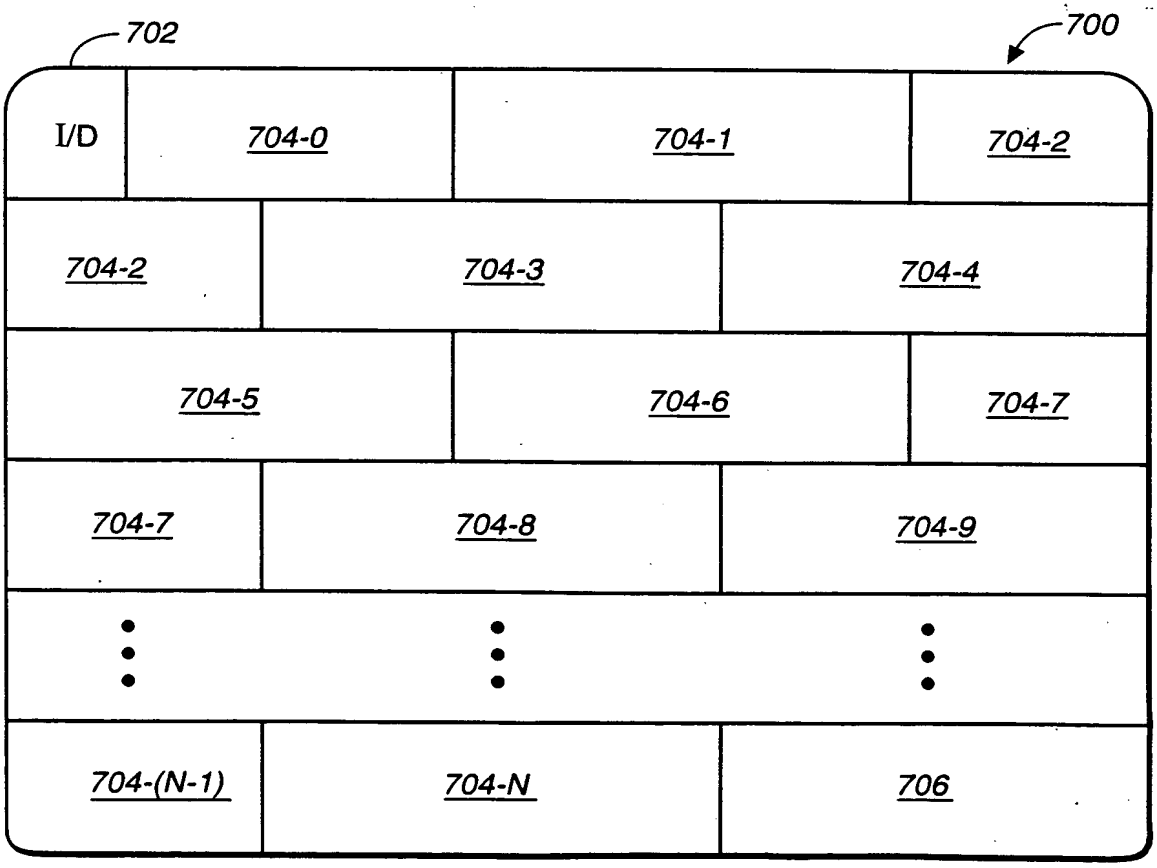

702
700
I/D
704-0
704-1
704-2
704-2
704-3
704-4
704-5
704-6
704-7
704-7
704-8
704-9
704-(N-1)
704-N
706

FIG._7

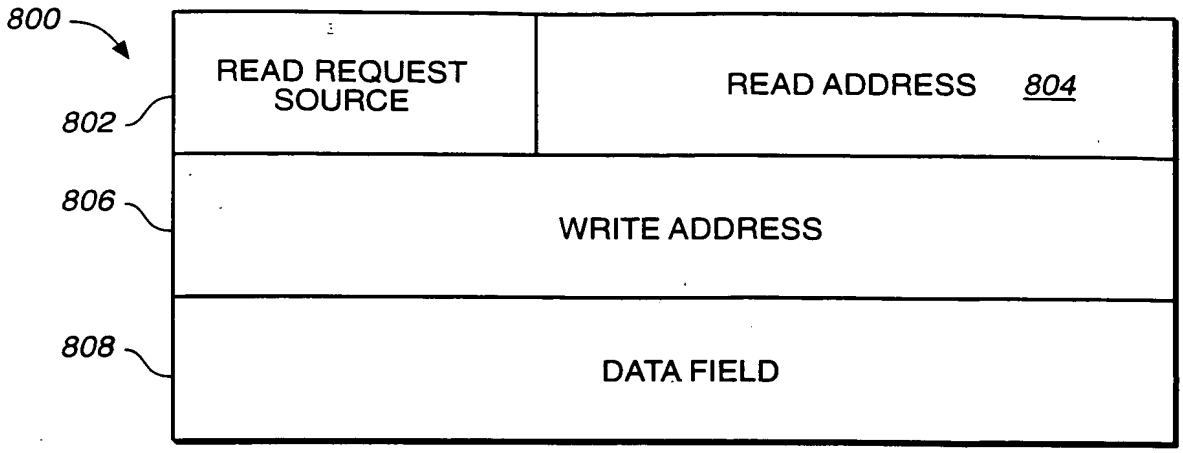

800
READ REQUEST SOURCE
READ ADDRESS 804
802
806
WRITE ADDRESS
808
DATA FIELD

FIG._8

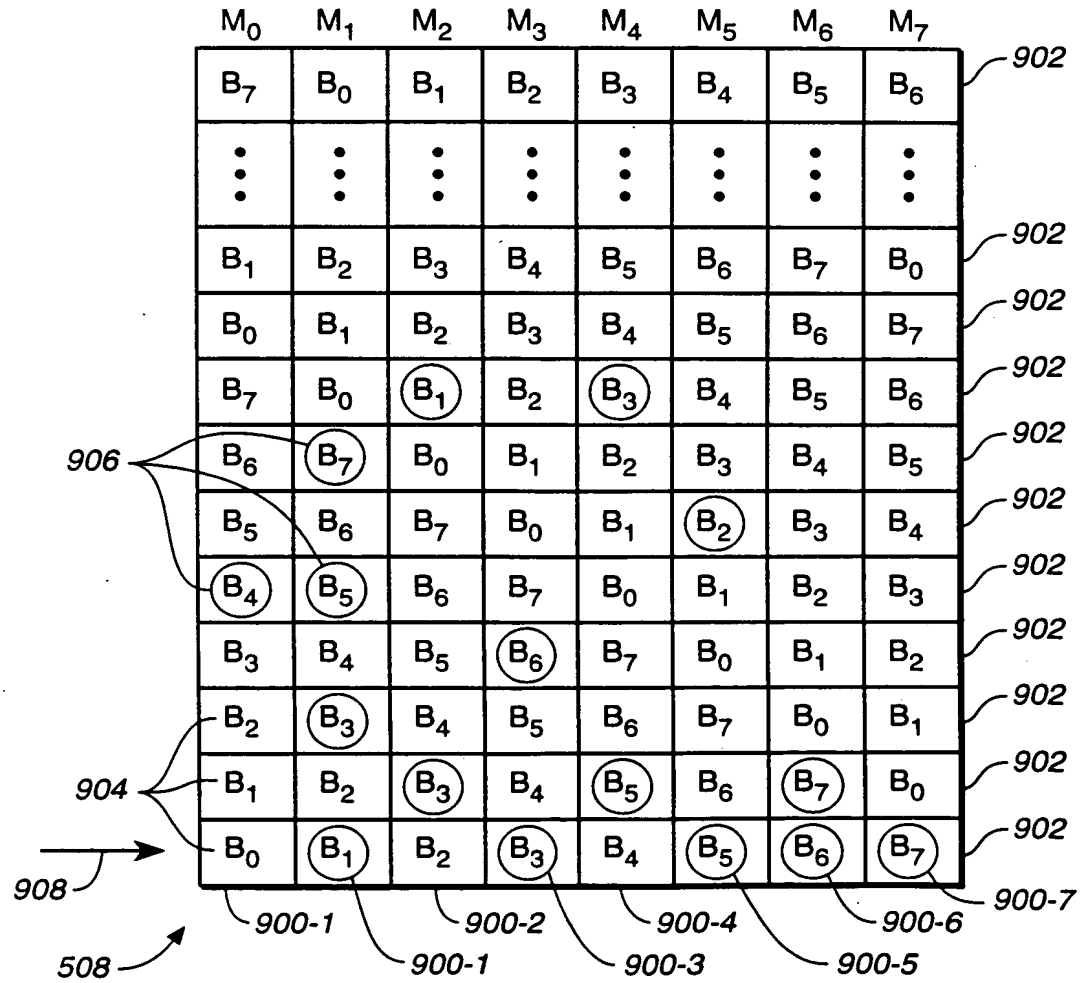

M0 M1 M2 M3 M4 M5 M6 M7
902
906
904
908
508
900-1
900-1
900-2
900-3
900-4
900-5
900-6
900-7

FIG._9

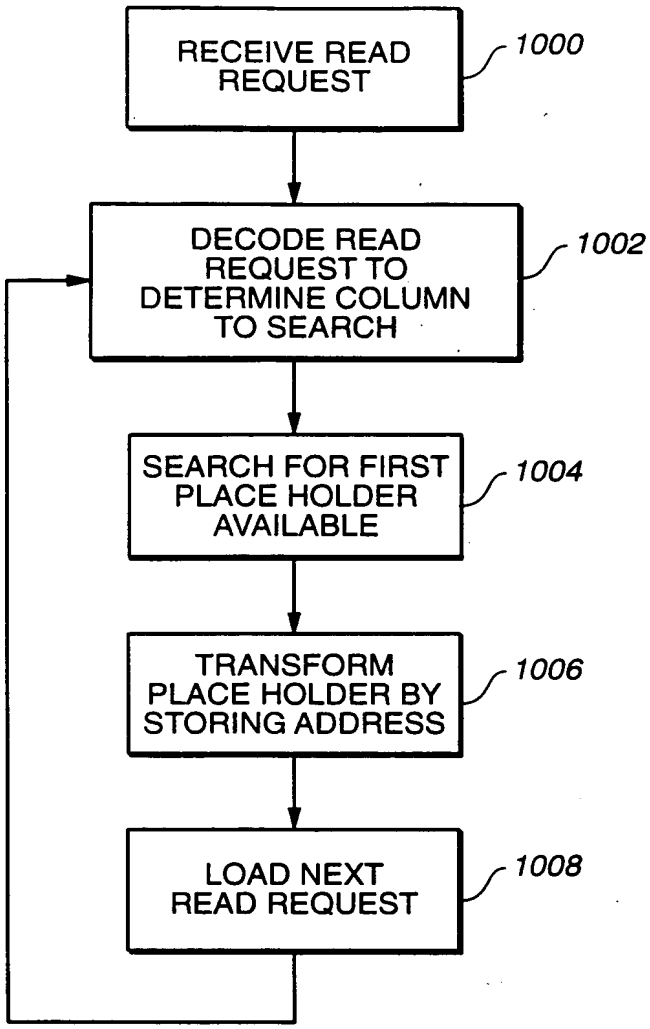

RECEIVE READ REQUEST
1000
DECODE READ REQUEST TO DETERMINE COLUMN TO SEARCH
1002
SEARCH FOR FIRST PLACE HOLDER AVAILABLE
1004
TRANSFORM PLACE HOLDER BY STORING ADDRESS
1006
LOAD NEXT READ REQUEST
1008

FIG._10

66C7EF n3853n60

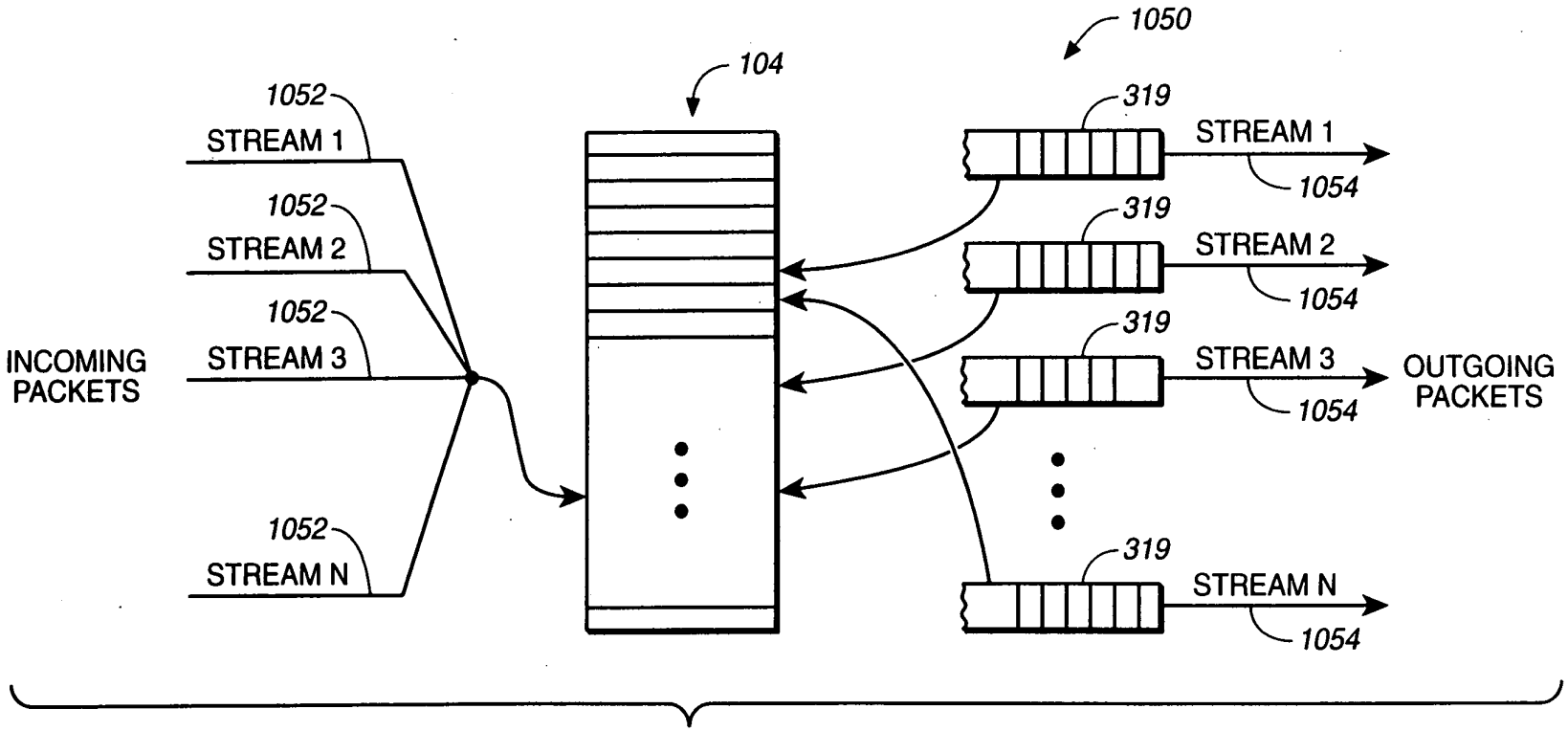


FIG._11A

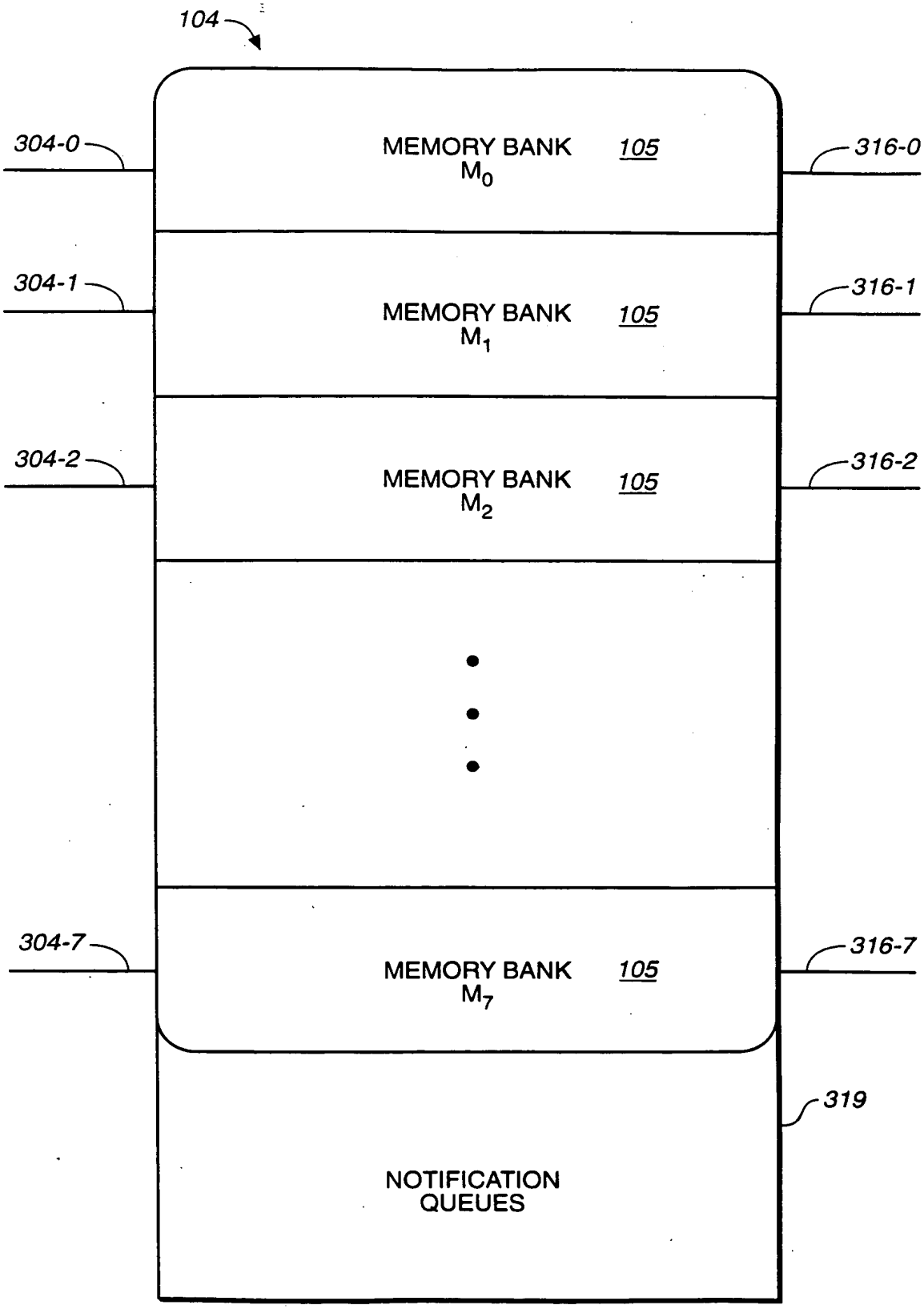

104
304-0
MEMORY BANK
M0
105
316-0
304-1
MEMORY BANK
M1
105
316-1
304-2
MEMORY BANK
M2
105
316-2
304-7
MEMORY BANK
M7
105
316-7
319
NOTIFICATION
QUEUES

FIG._11B

6621271 1989960

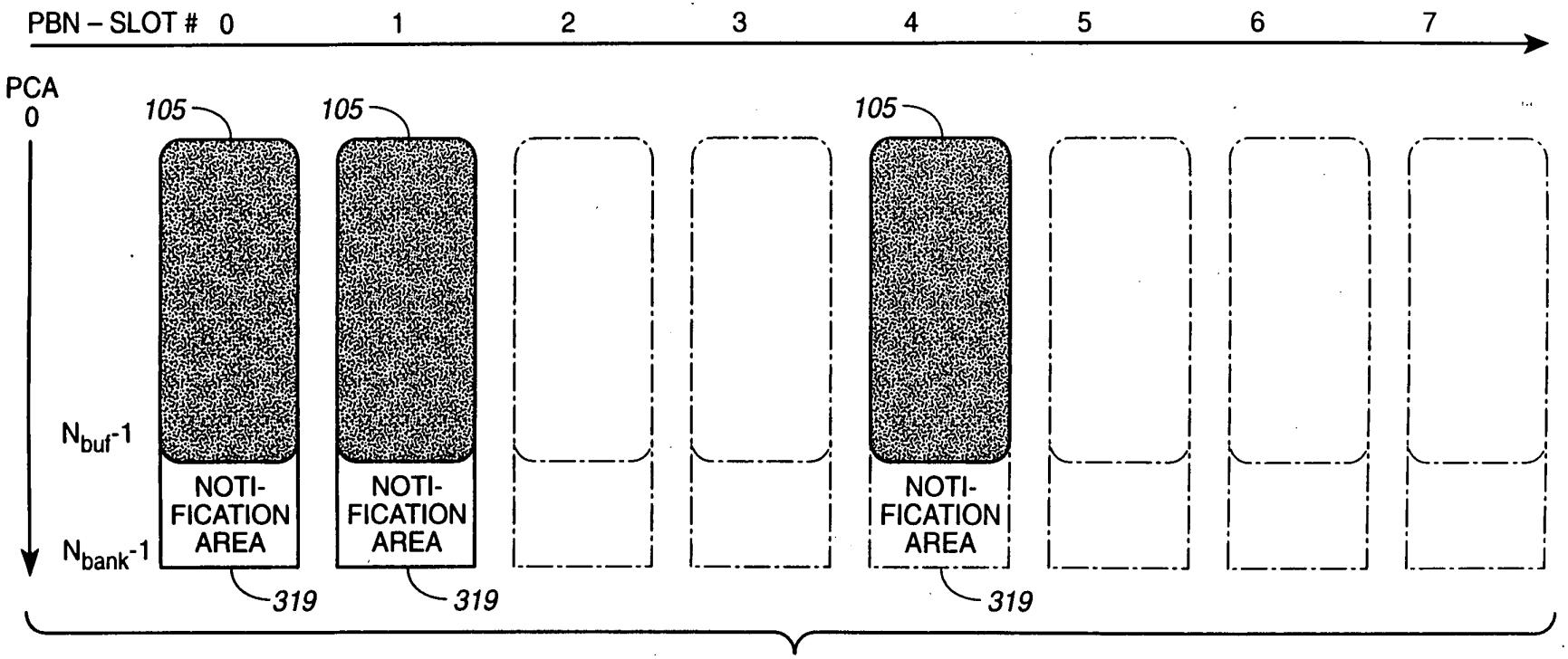


FIG._11C

6627627 1989960

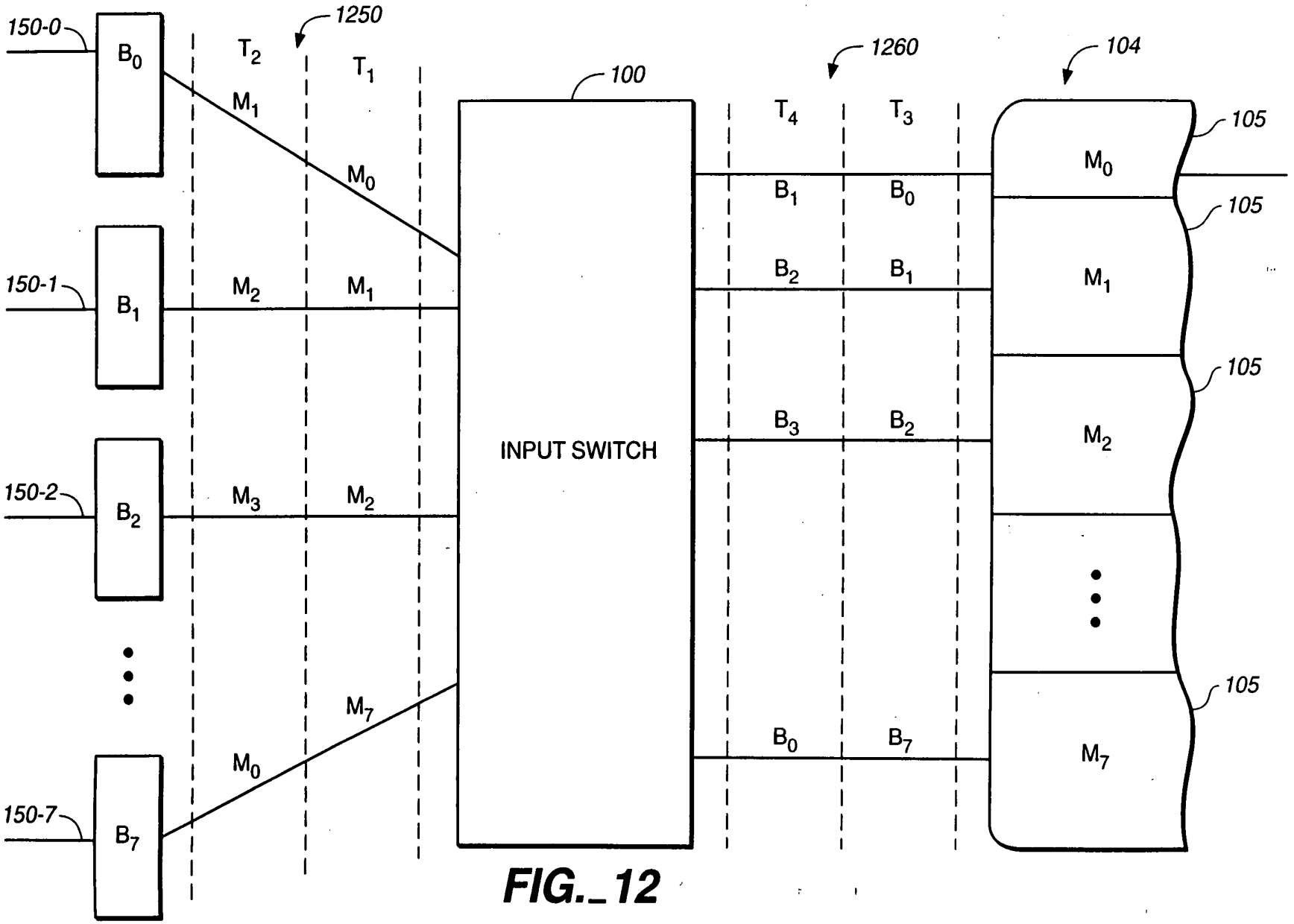


FIG._12

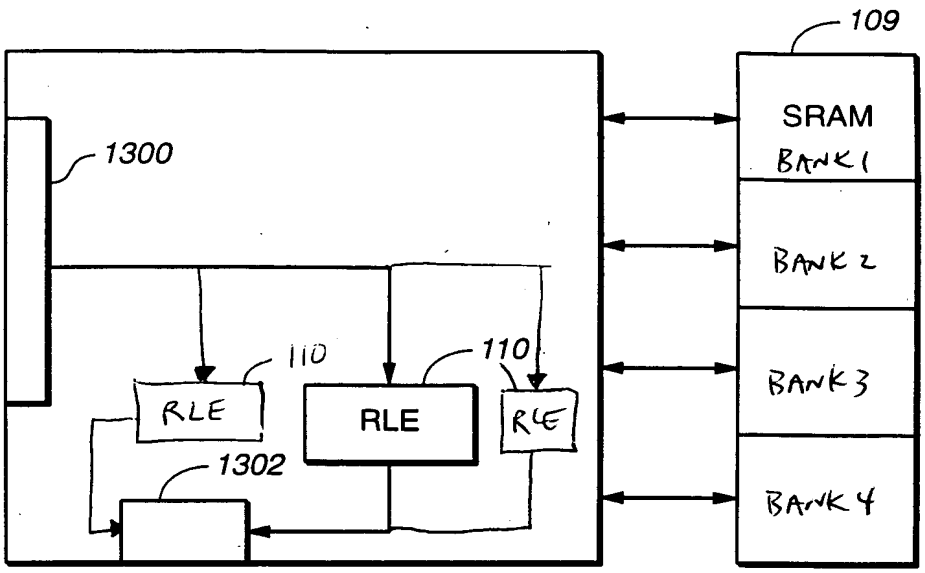


FIG._13A

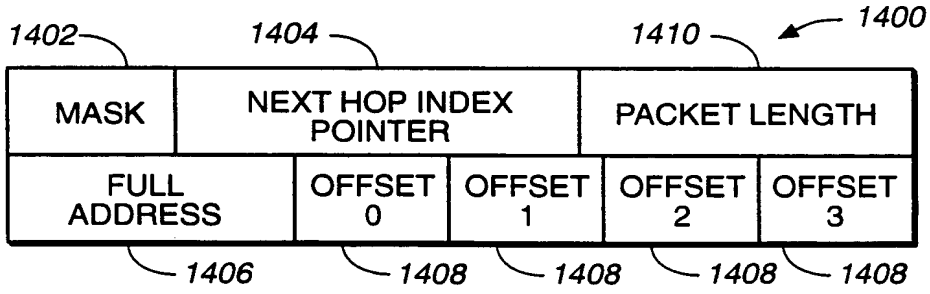


FIG._14

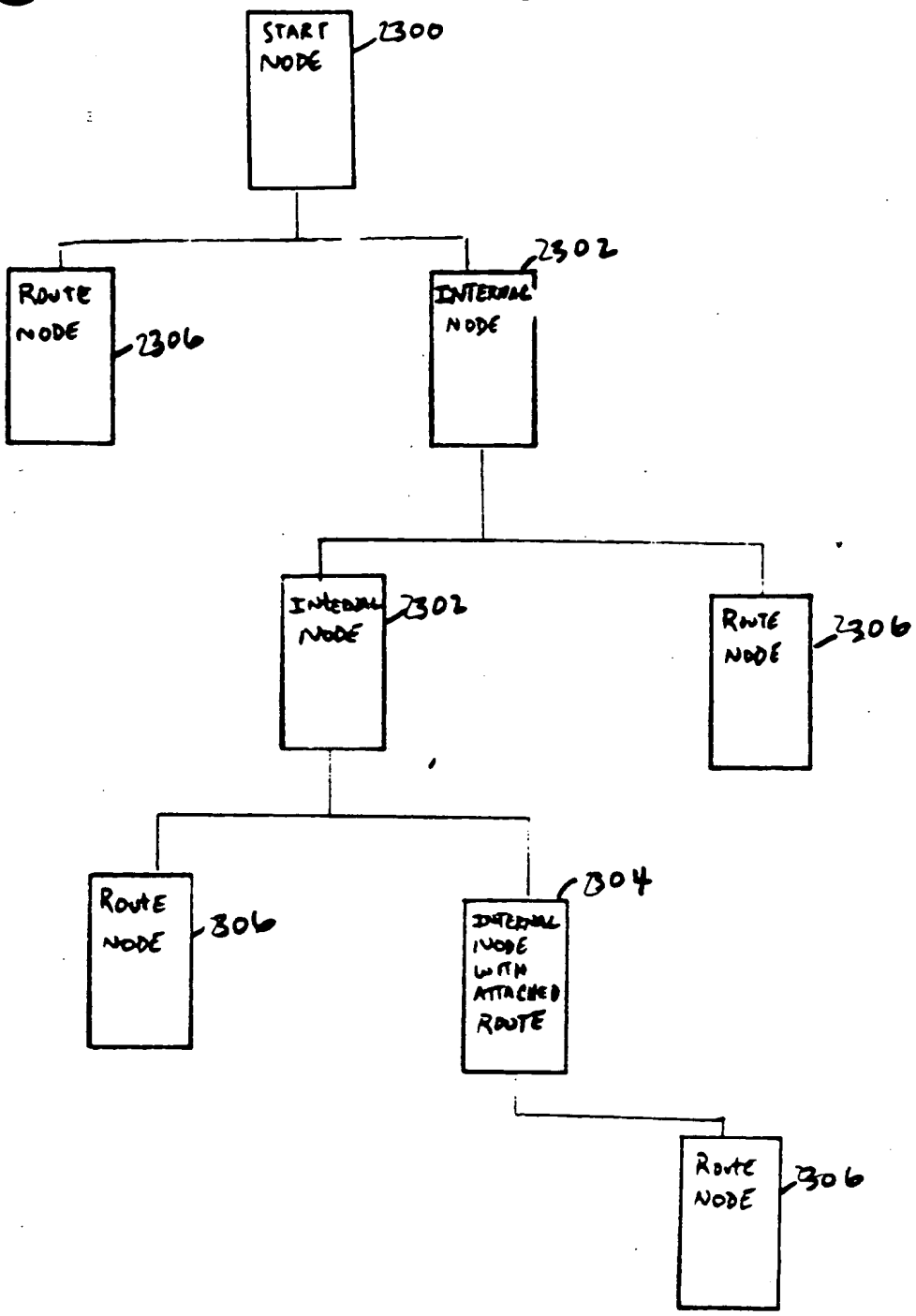
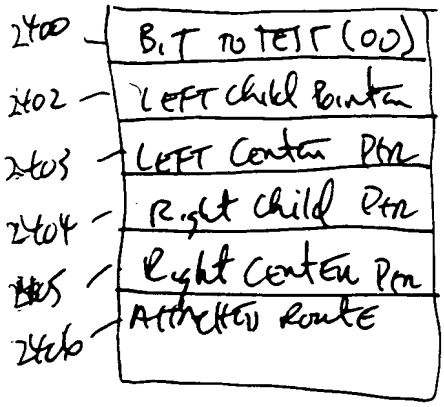

START NODE
2300
ROUTE NODE
2306
INTERNAL NODE
2302
INTERNAL NODE
2302
ROUTE NODE
2306
ROUTE NODE
306
INTERNAL NODE WITH ATTACHED ROUTE
304
ROUTE NODE
306

FIGURE 3B



13 D

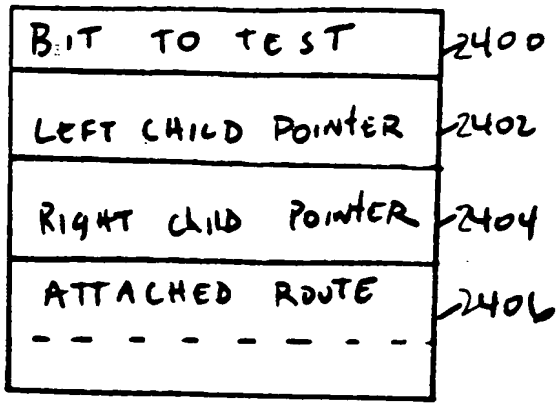


FIGURE 13C

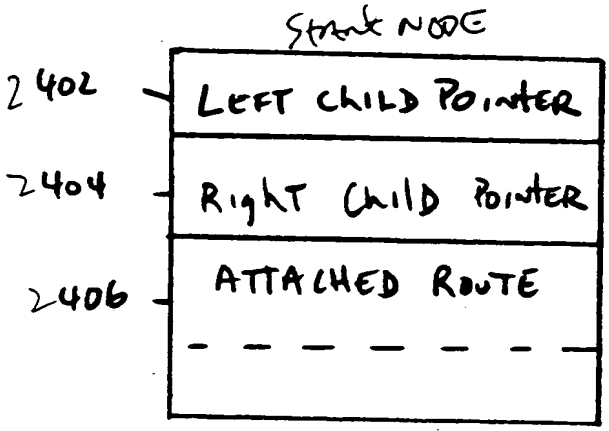


FIGURE 13E

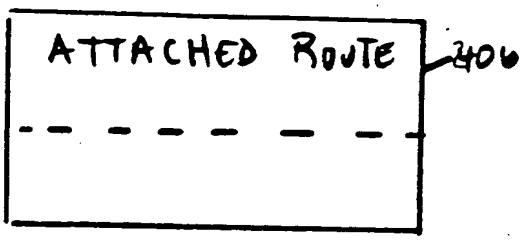


FIGURE 13F

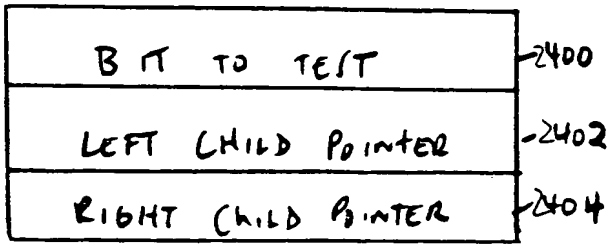


FIGURE 13G

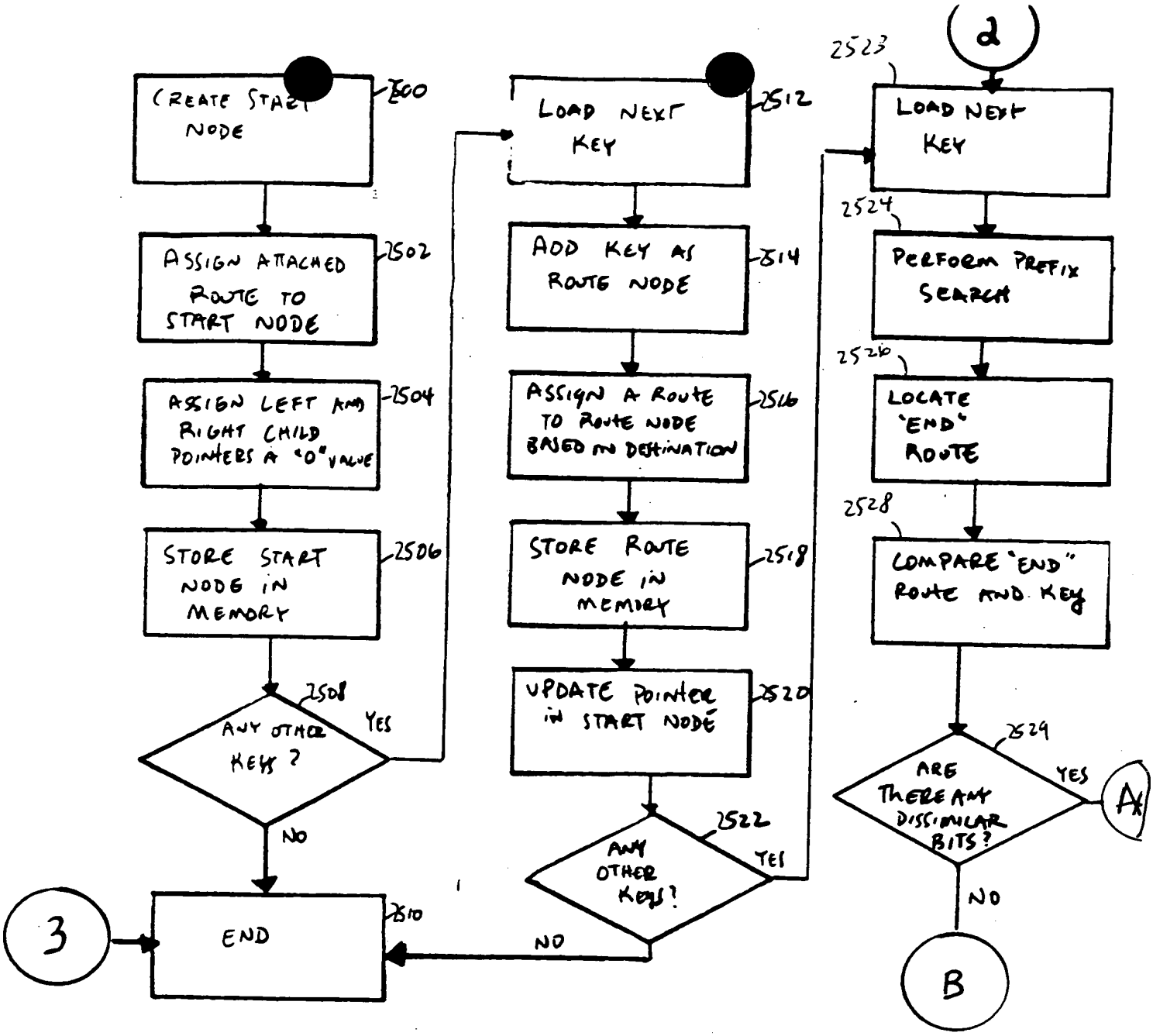

CREATE START NODE
2500
ASSIGN ATTACHED ROUTE TO START NODE
2502
ASSIGN LEFT AND RIGHT CHILD POINTERS A "0" VALUE
2504
STORE START NODE IN MEMORY
2506
ANY OTHER KEYS ?
2508
YES
NO
END
2510
3
LOAD NEXT KEY
2512
ADD KEY AS ROUTE NODE
2514
ASSIGN A ROUTE TO ROUTE NODE BASED ON DESTINATION
2516
STORE ROUTE NODE IN MEMORY
2518
UPDATE POINTER IN START NODE
2520
ANY OTHER KEYS?
2522
YES
NO
2523
2
LOAD NEXT KEY
2524
PERFORM PREFIX SEARCH
2526
LOCATE "END" ROUTE
2528
COMPARE "END" ROUTE AND KEY
2529
ARE THERE ANY DISSIMILAR BITS?
YES
NO
A
B

FIGURE 13H

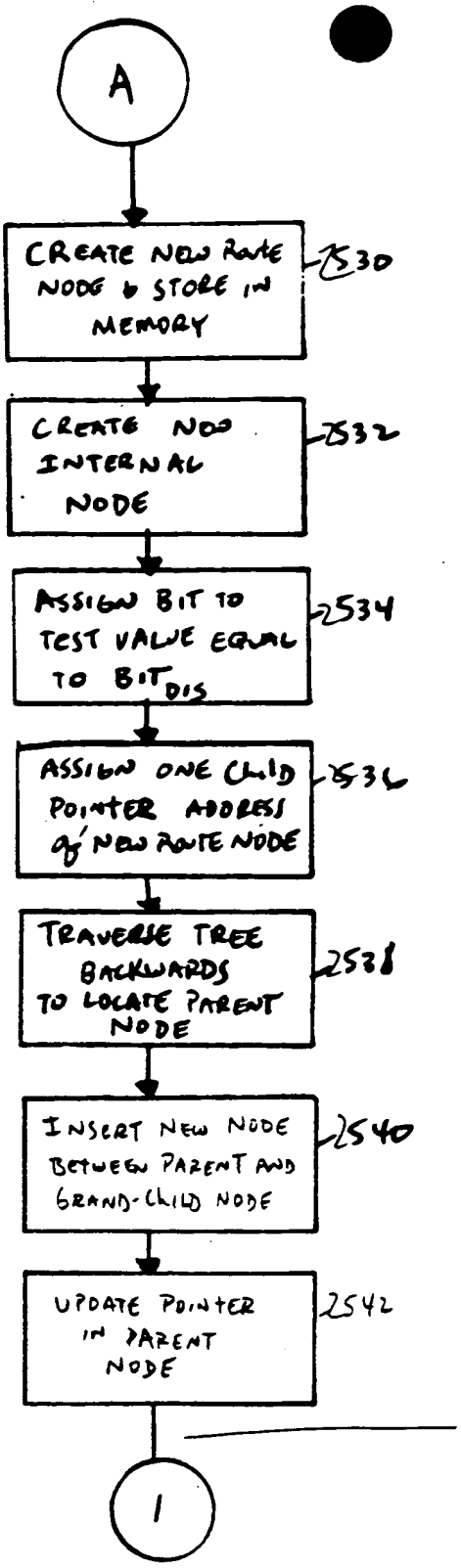

A
CREATE NEW ROUTE NODE & STORE IN MEMORY
2530
CREATE NON INTERNAL NODE
2532
ASSIGN BIT TO TEST VALUE EQUAL TO BIT DIS
2534
ASSIGN ONE CHILD POINTER ADDRESS OF NEW ROUTE NODE
2536
TRAVERSE TREE BACKWARDS TO LOCATE PARENT NODE
2538
INSERT NEW NODE BETWEEN PARENT AND GRAND-CHILD NODE
2540
UPDATE POINTER IN PARENT NODE
2542
1

FIGURE 13I

0055555 .4140

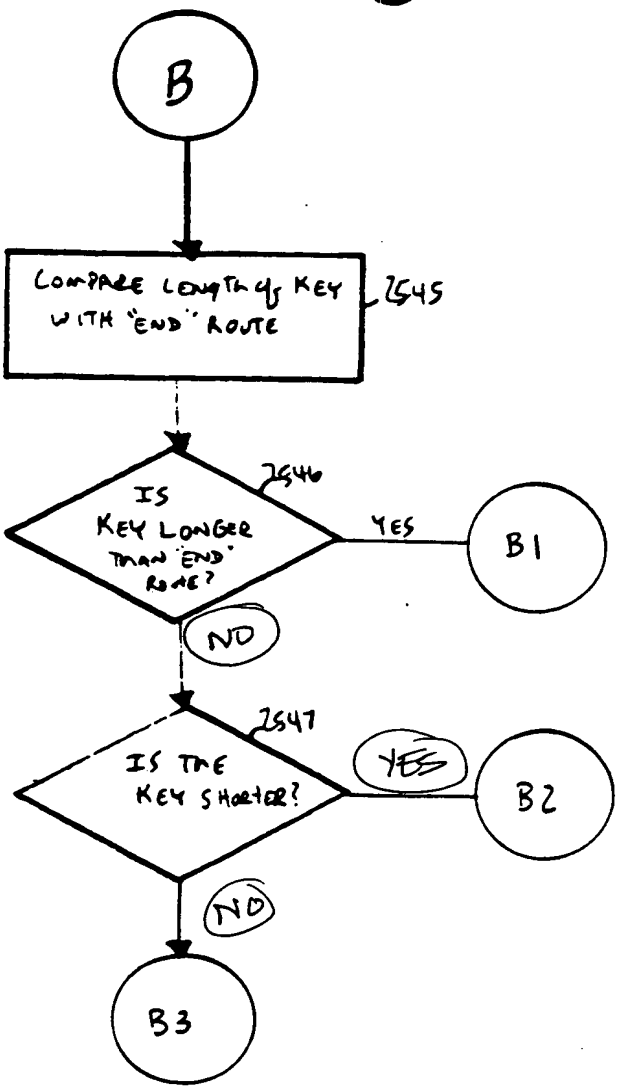


FIGURE 13J.

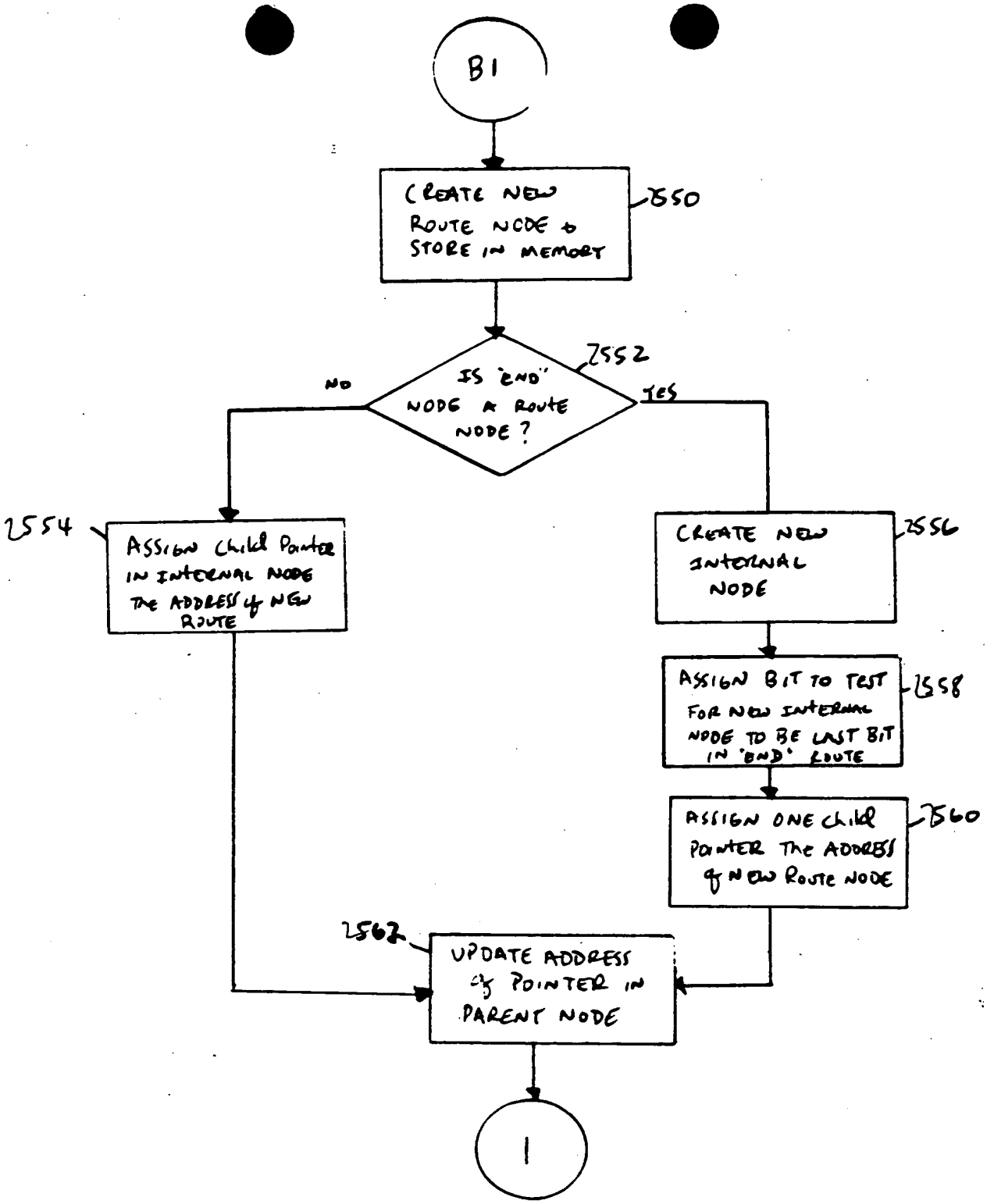


FIGURE 13K

D95950 4P2P 05

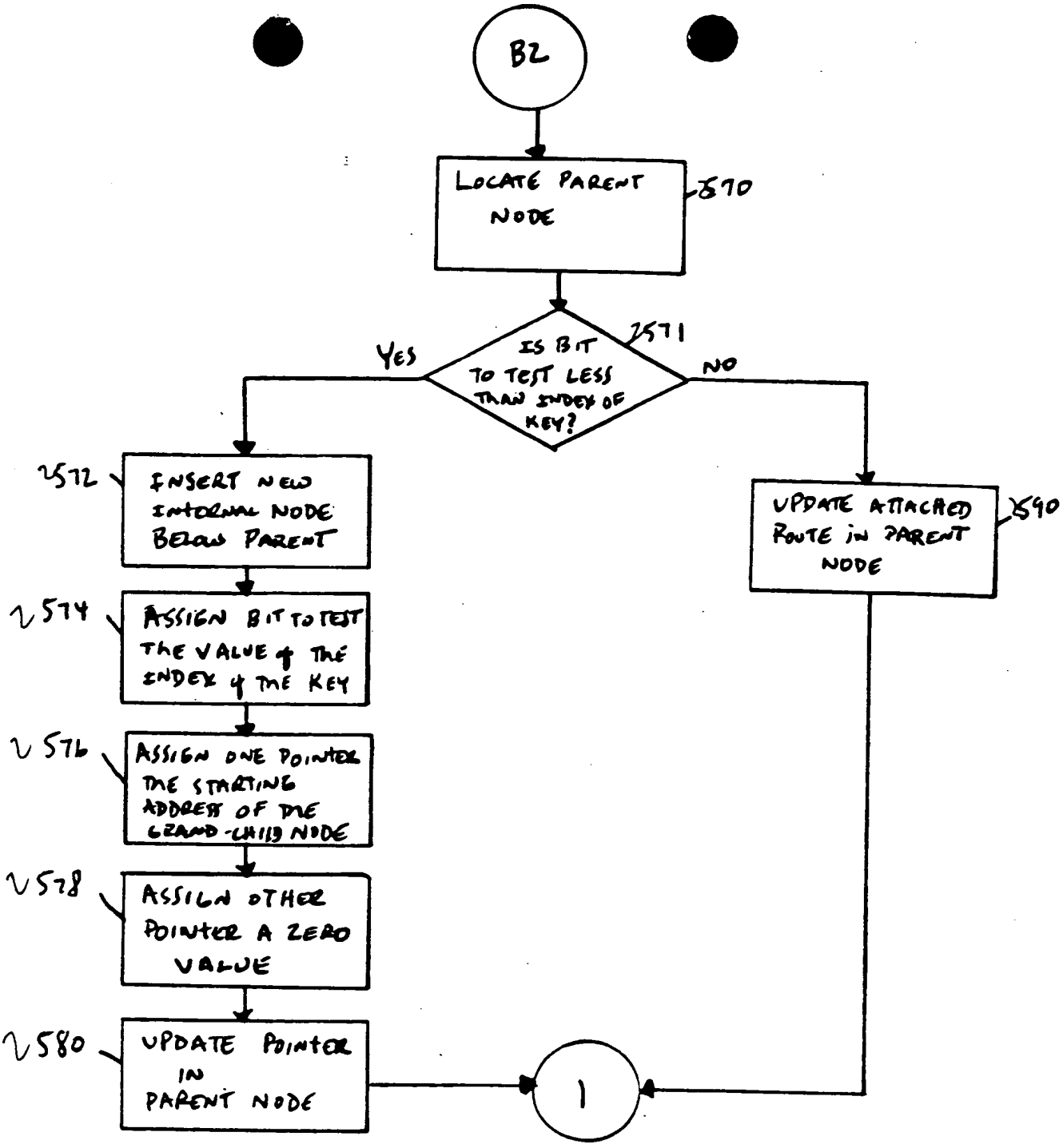

B2
LOCATE PARENT NODE
570
IS BIT TO TEST LESS THAN INDEX OF KEY?
571
YES
NO
572
INSERT NEW INTERNAL NODE BELOW PARENT
574
ASSIGN BIT TO TEST THE VALUE of THE INDEX of THE KEY
576
ASSIGN ONE POINTER THE STARTING ADDRESS OF THE GRAND-CHILD NODE
578
ASSIGN OTHER POINTER A ZERO VALUE
580
UPDATE POINTER IN PARENT NODE
590
UPDATE ATTACHED ROUTE in PARENT NODE
1

FIGURE 13L

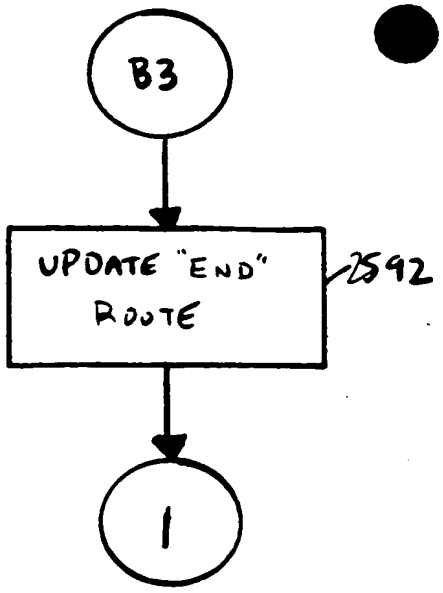


FIGURE 13M

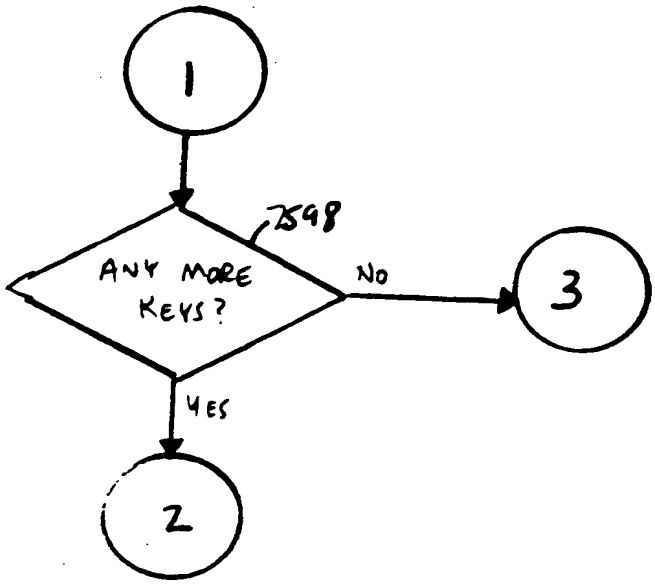


FIGURE 13N

Document: 1 of 1

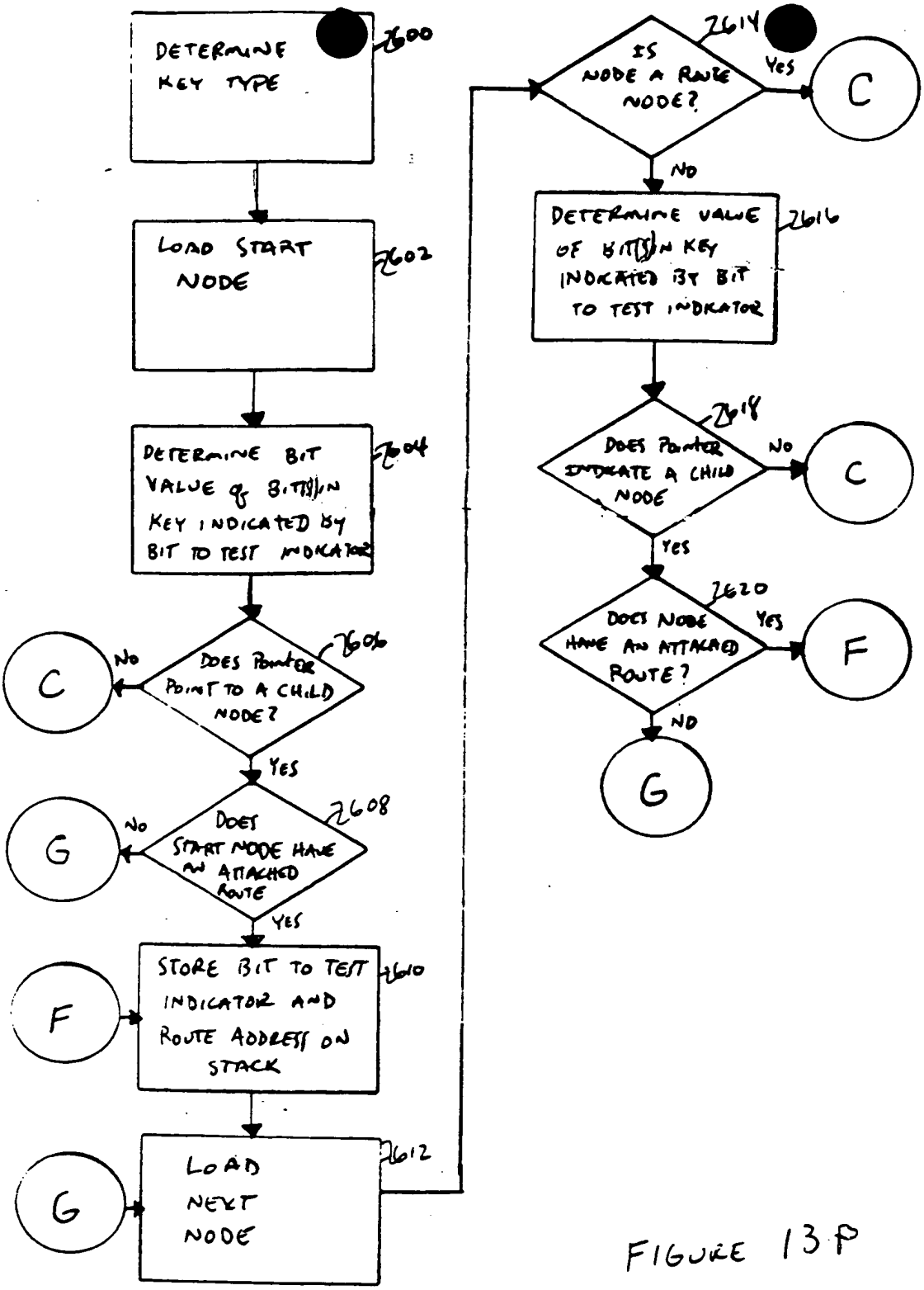

DETERMINE KEY TYPE
2600
LOAD START NODE
2602
DETERMINE BIT VALUE OF BIT(S) IN KEY INDICATED BY BIT TO TEST INDICATOR
2604
DOES POINTER POINT TO A CHILD NODE?
2606
No
Yes
C
DOES START NODE HAVE AN ATTACHED ROUTE
2608
No
Yes
G
STORE BIT TO TEST INDICATOR AND ROUTE ADDRESS ON STACK
2610
F
LOAD NEXT NODE
2612
G
IS NODE A ROUTE NODE?
2614
Yes
No
C
DETERMINE VALUE OF BIT(S) IN KEY INDICATED BY BIT TO TEST INDICATOR
2616
DOES POINTER INDICATE A CHILD NODE
2618
No
Yes
C
DOES NODE HAVE AN ATTACHED ROUTE?
2620
Yes
No
F
G

FIGURE 13P

Docket No. 1-1-1-1-1-1

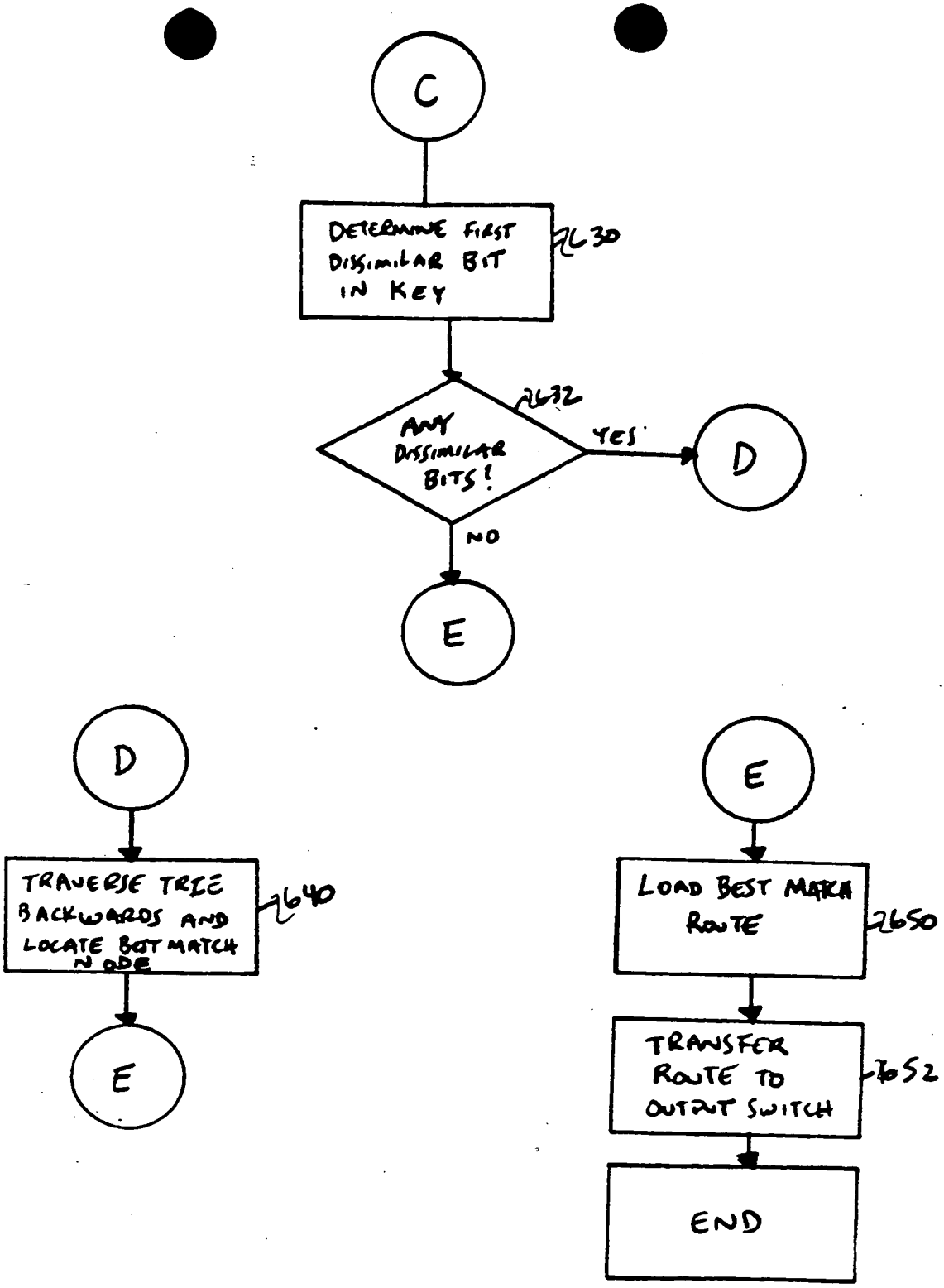


FIGURE 13Q

66C12F "9899160

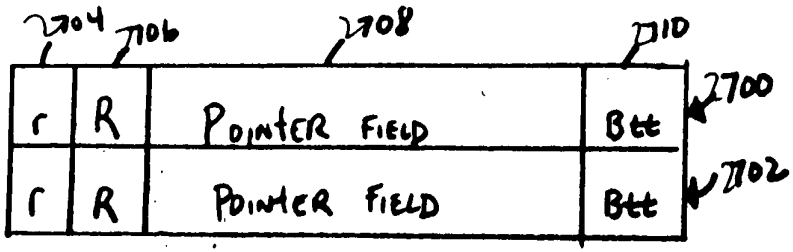


FIGURE 13R

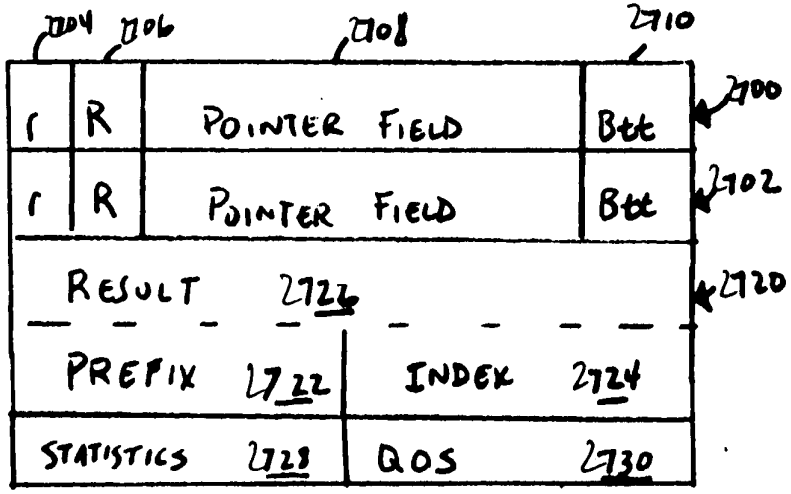


FIGURE 13S

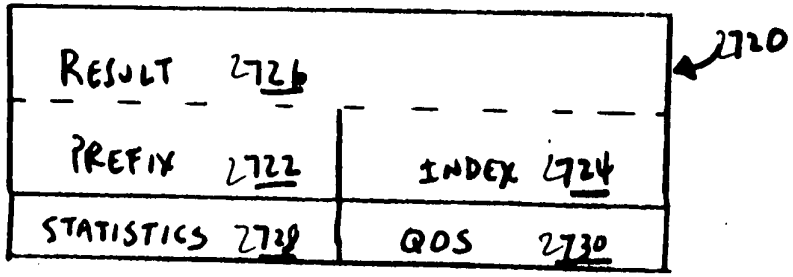
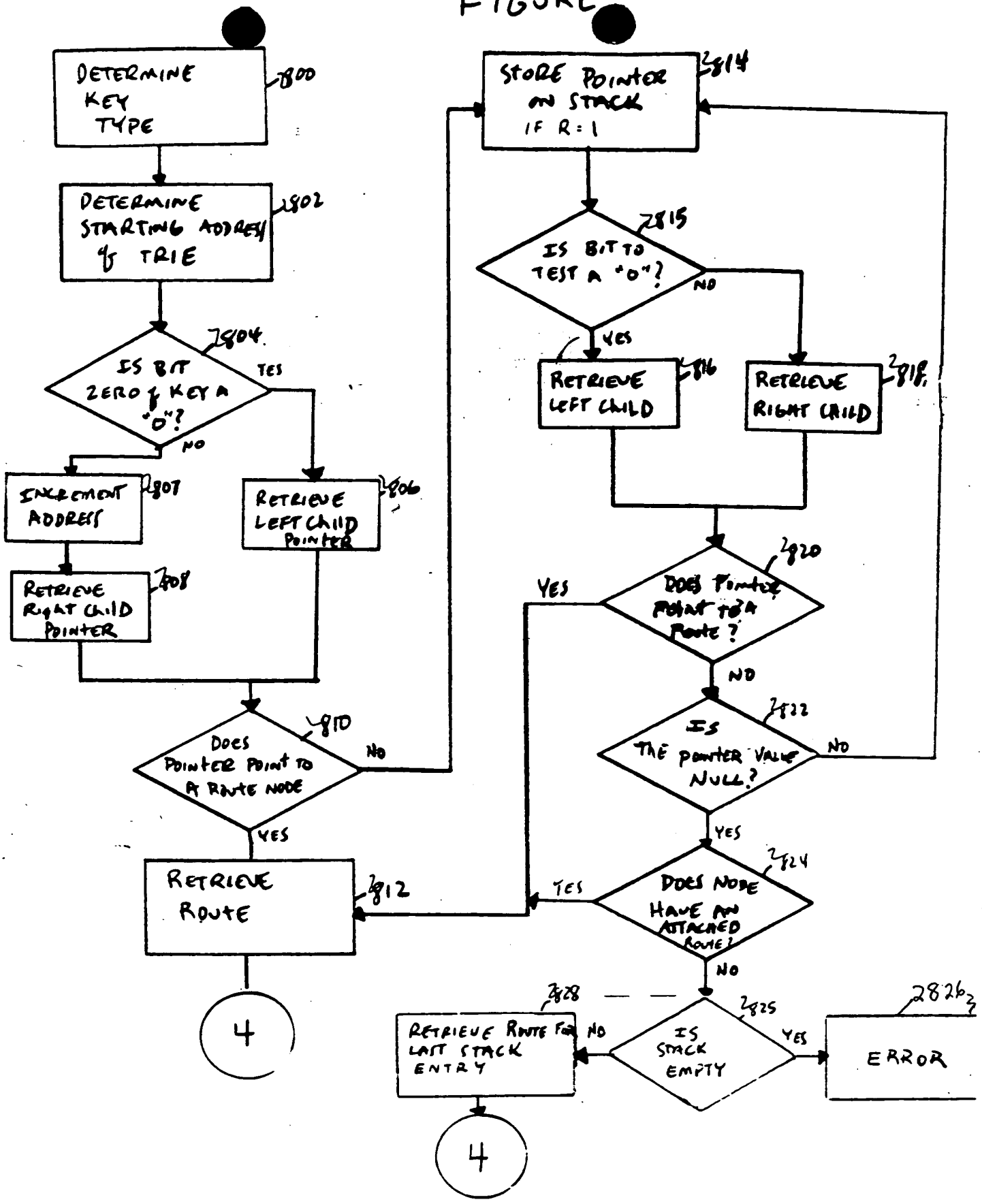


FIGURE 13T

FIGURE


DETERMINE KEY TYPE
800
DETERMINE STARTING ADDRESS of TRIE
802
IS BIT ZERO of KEY a "0"?
804
YES
NO
INCREMENT ADDRESS
807
RETRIEVE LEFT CHILD POINTER
806
RETRIEVE Right CHILD POINTER
808
DOES POINTER POINT TO A ROUTE NODE
810
NO
YES
RETRIEVE ROUTE
812
4
STORE POINTER ON STACK IF R=1
814
IS BIT TO TEST A "0"?
815
YES
NO
RETRIEVE LEFT CHILD
816
RETRIEVE RIGHT CHILD
818
DOES Pointer Point to A Route ?
820
YES
NO
IS THE POINTER VALUE NULL?
822
NO
YES
DOES NODE HAVE AN ATTACHED ROUTE?
824
YES
NO
IS STACK EMPTY
825
YES
NO
ERROR
826
RETRIEVE ROUTE FOR LAST STACK ENTRY
828
4

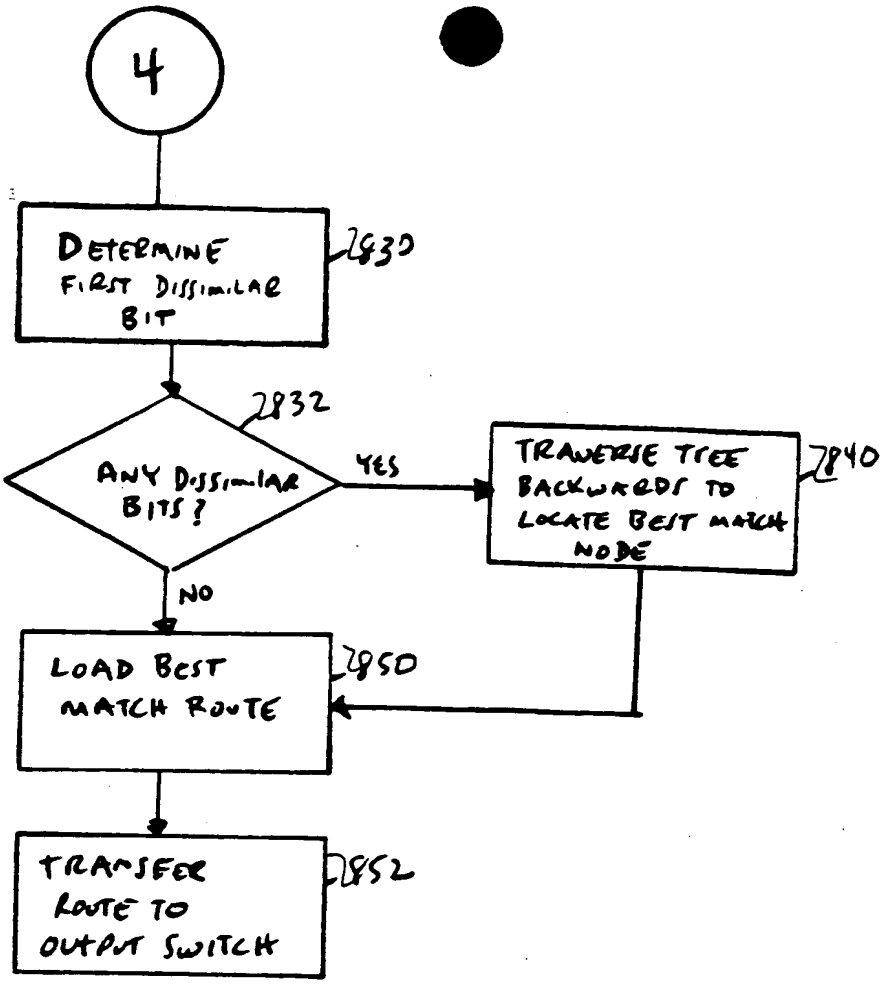


FIGURE ~~8~~B 13 V

DOCUMENT NUMBER

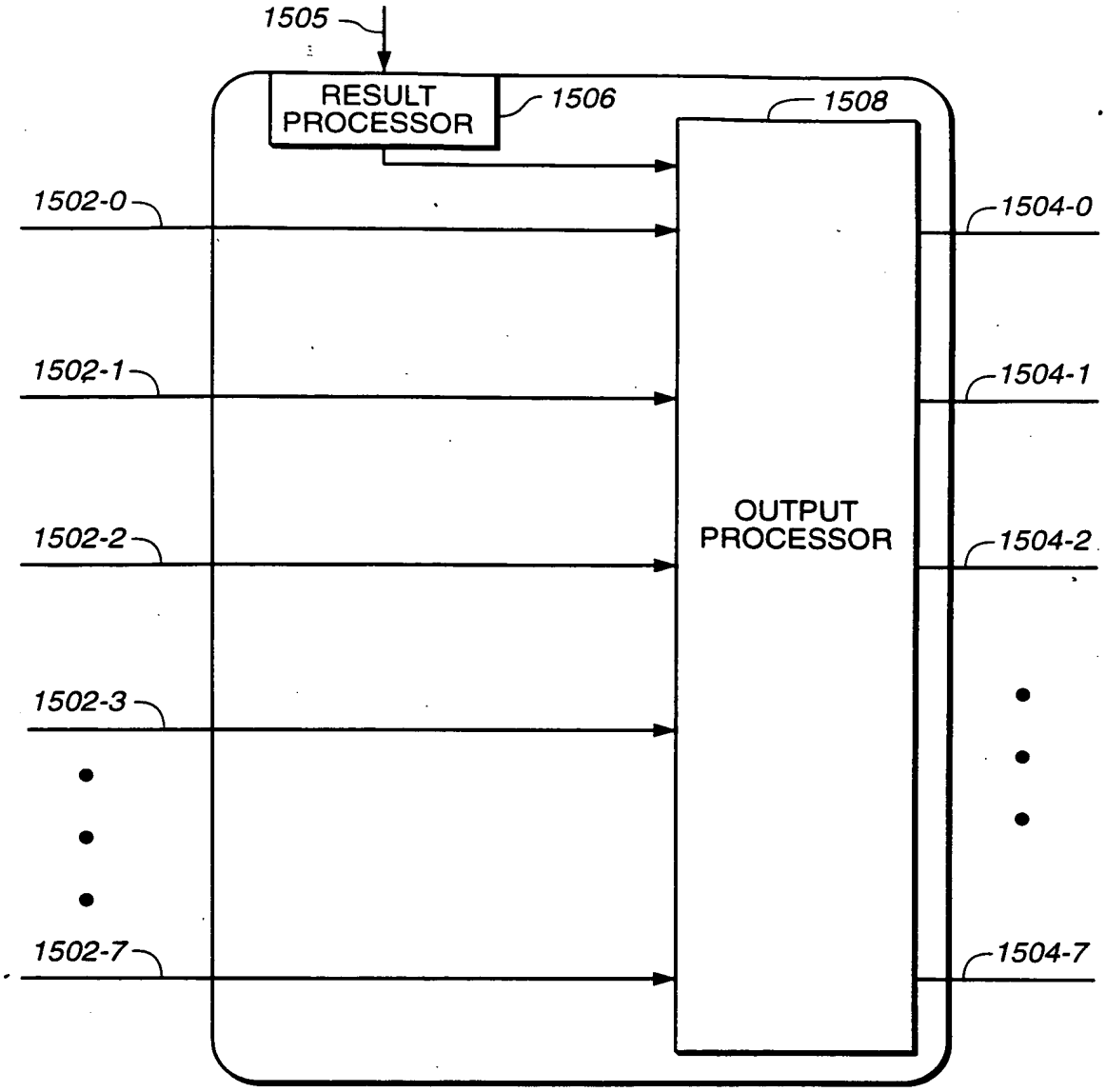


FIG._15A

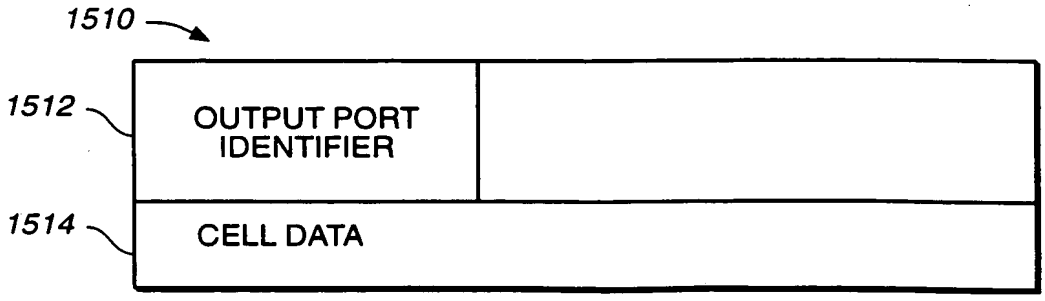


FIG._15B

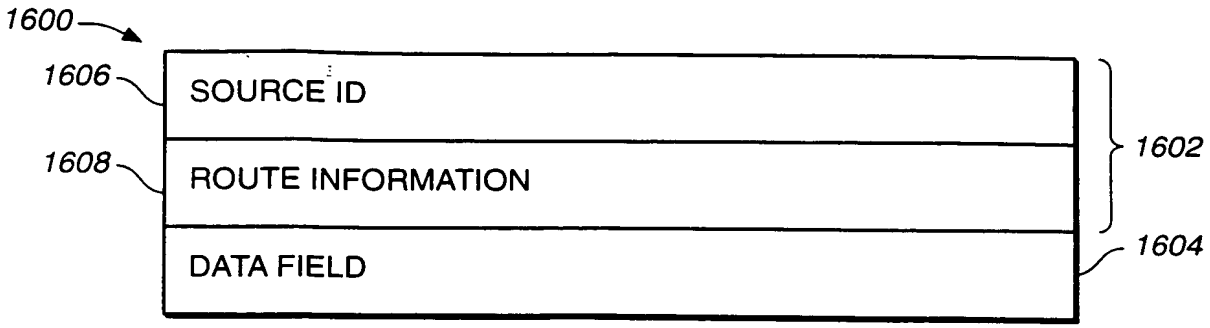


FIG._16

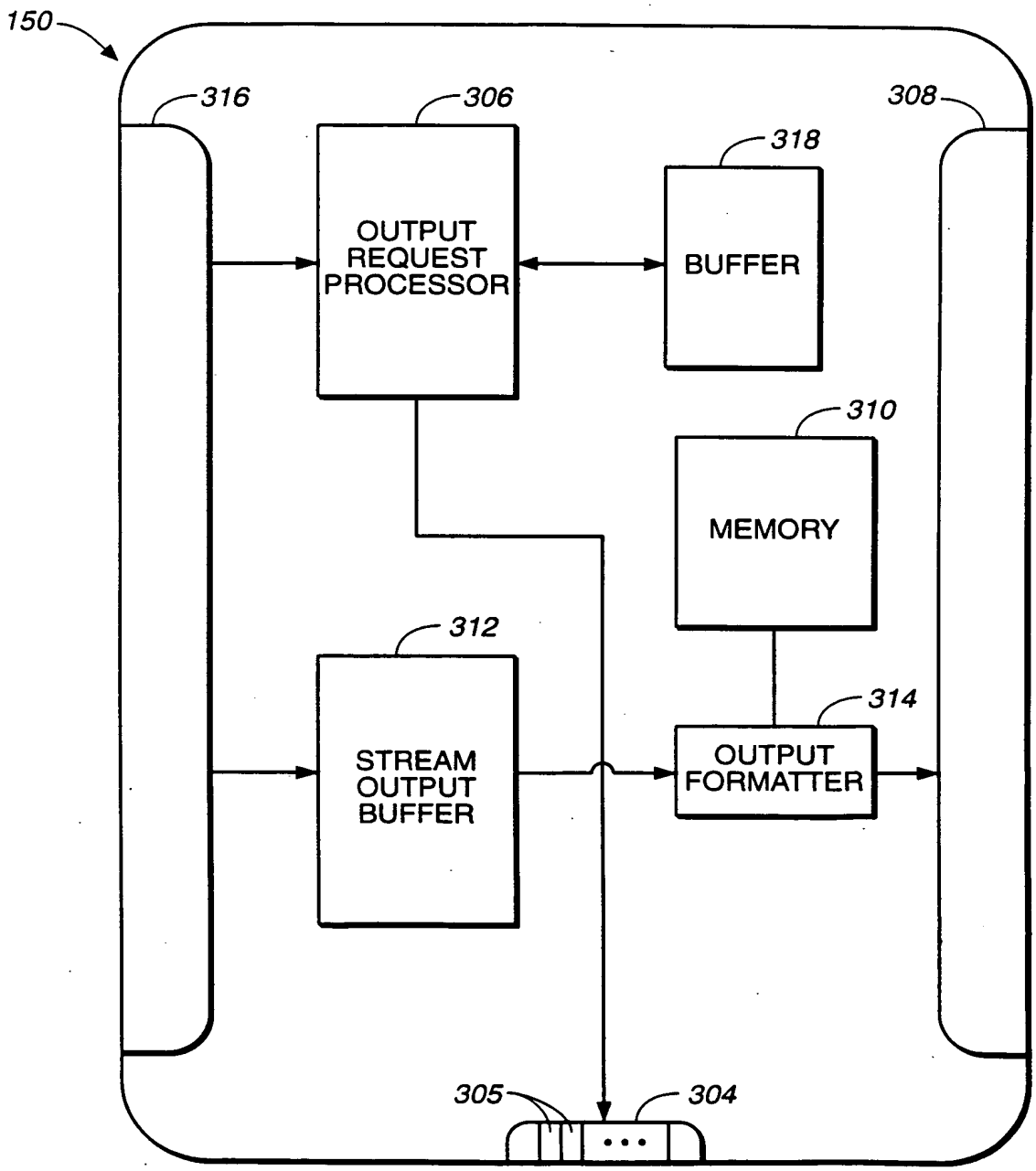


FIG._17A

6627271 1999960

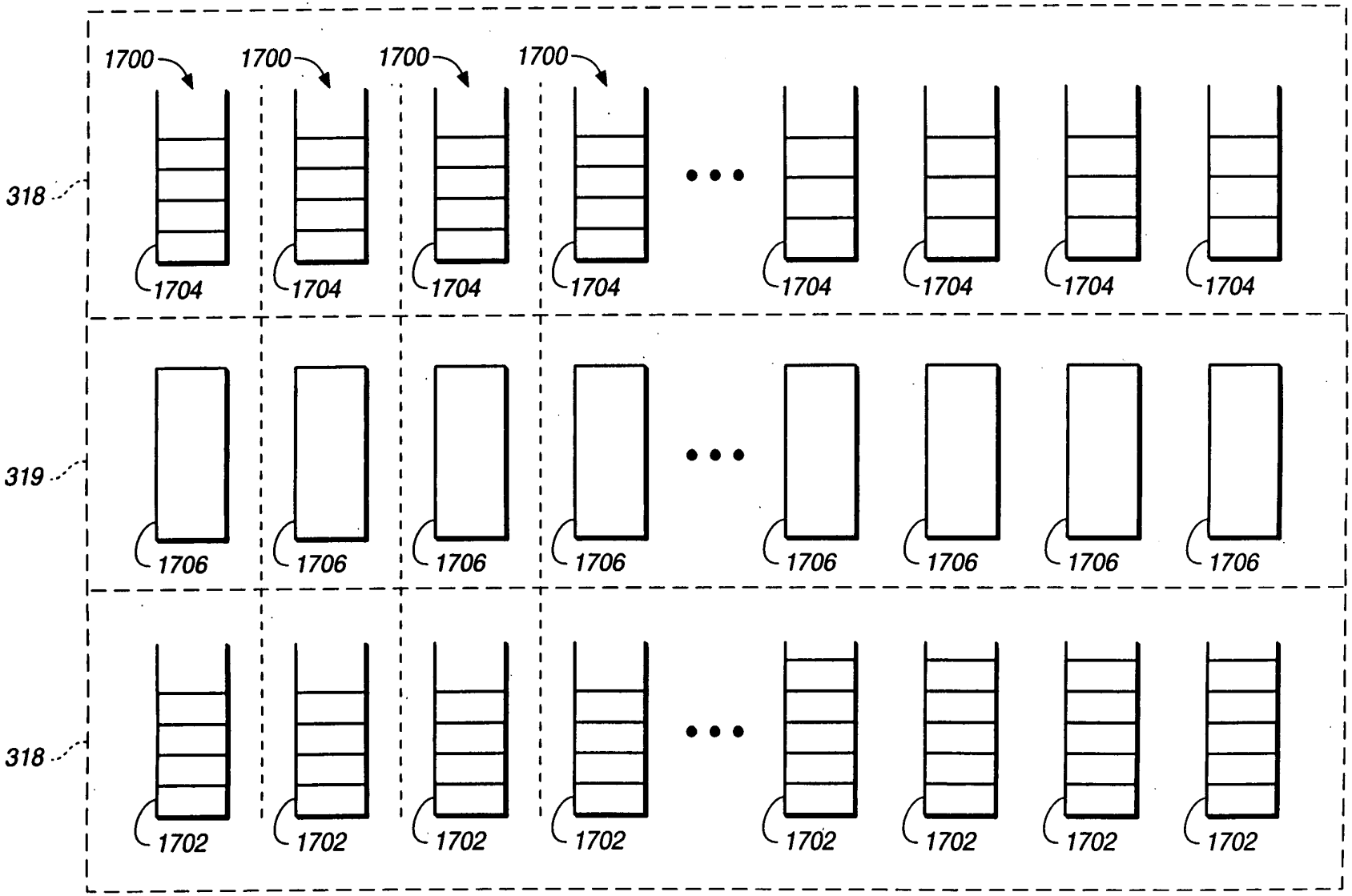


FIG._17B

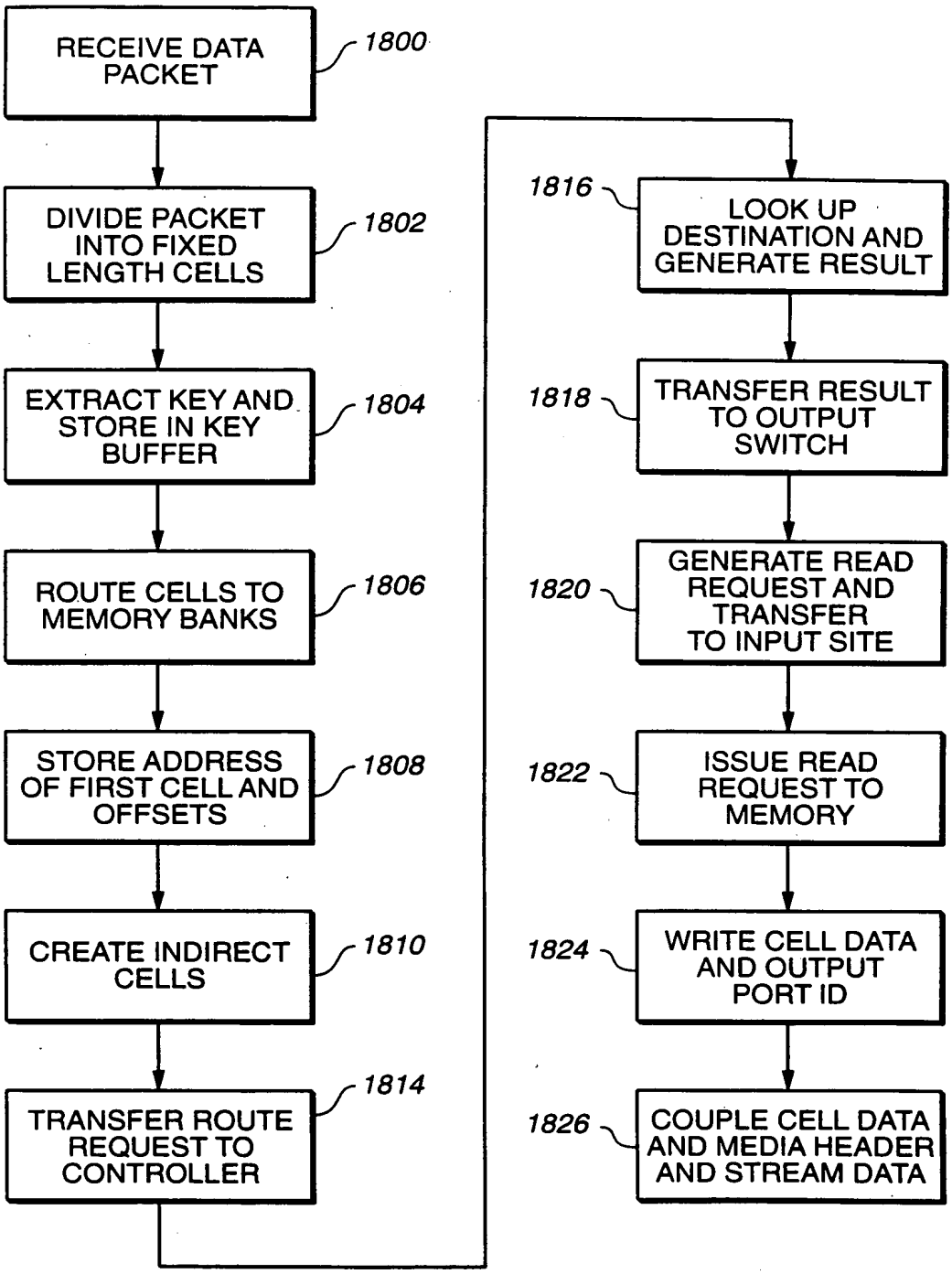

RECEIVE DATA PACKET
1800
DIVIDE PACKET INTO FIXED LENGTH CELLS
1802
EXTRACT KEY AND STORE IN KEY BUFFER
1804
ROUTE CELLS TO MEMORY BANKS
1806
STORE ADDRESS OF FIRST CELL AND OFFSETS
1808
CREATE INDIRECT CELLS
1810
TRANSFER ROUTE REQUEST TO CONTROLLER
1814
1816
LOOK UP DESTINATION AND GENERATE RESULT
1818
TRANSFER RESULT TO OUTPUT SWITCH
1820
GENERATE READ REQUEST AND TRANSFER TO INPUT SITE
1822
ISSUE READ REQUEST TO MEMORY
1824
WRITE CELL DATA AND OUTPUT PORT ID
1826
COUPLE CELL DATA AND MEDIA HEADER AND STREAM DATA

FIG._18